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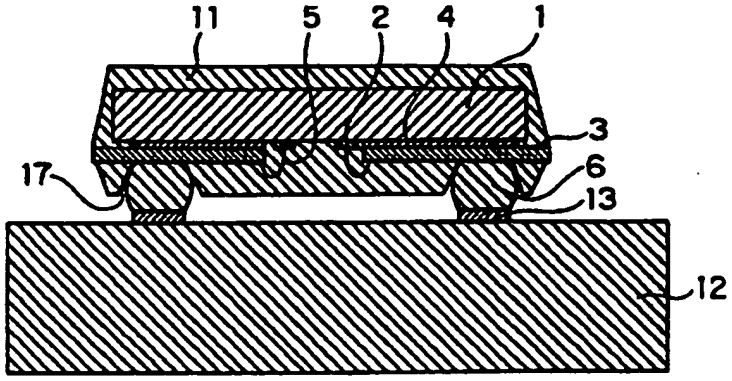
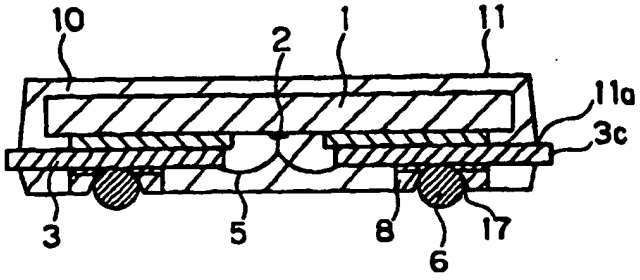
(54) Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

(57) Abstract

A semiconductor device comprises a semiconductor element (1) having a plane (1a) with a plurality of electrodes (2) formed thereon, a plurality of internal leads (3; 20) electrically connected to the electrodes (2) respectively, and an electrically insulating resin package (11) for sealing the semiconductor element (1) and the internal leads (3; 20), wherein the internal leads (3; 20) are substantially located in the range of the electrode formed plane (1a) and the resin package (11) has a plurality of external terminal receiving recesses (17) reaching the internal leads (3; 20) respectively in the range of said electrode formed plane (1a). The external terminal receiving recesses (17) is formed by a resin plate (8) having through-holes and integrally molded with the resin package (11). The resin plate (8) may have recesses (18) and film members (19) forming the bottom of said recesses (18) and to be broken after integrally molded with the resin package (11).





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DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

TECHNICAL FIELD

The present invention relates to a resin-sealed semiconductor device, particularly to a semiconductor device in which external terminals are formed in an area of a surface of a semiconductor element on which electrodes are formed and method of manufacturing the same.

BACKGROUND ART

While the integration level of a semiconductor device is further raised, an art for making the plane size of a semiconductor device approach the plane size of a semiconductor element is developed. This art includes two types one of which is referred to as the bare chip mounting. This is a method for forming a structure in which a semiconductor element is directly joined to a printed circuit board by bumps and sealed by resin.

The other is a method for decreasing the size of a resin package in which a semiconductor element is sealed up to the plane size of the semiconductor element as possible. This method is generally referred to as a CSP (abbreviation of a chip siz package or chip scal package).

Some of the CSP structures are disclosed in Japanese Patent Unexamined Publication No. 6-224259, WO 92/05582 Publication, Japanese Patent Unexamined Publication No. 6-302604, and Japanese Patent Unexamined Publication No. 6-132453. Japanese Patent Unexamined Publication No. 6-224259 discloses a CSP structure in which a semiconductor element is mounted on a ceramic substrate provided with through-holes and external terminals are formed on the opposite side of the ceramic substrate to mount the substrate on a printed circuit board. WO 92/05582 Publication discloses a CSP structure in which a tape with external terminals is applied on the electrode formed plane of a semiconductor element through a flexible material and the external terminals are electrically connected with electrodes of the semiconductor element. Moreover, Japanese Patent Unexamined Publication No. 6-302604 discloses a CSP structure in which a metallic wiring pattern is formed on the electrode formed plane of a semiconductor element and external terminals are formed on the pattern. Furthermore, Japanese Patent Unexamined Publication No. 6-132453 discloses a CSP structure in which leads bonded to an electrode forming surface of a semiconductor element are connected with electrodes and a part of the leads are exposed from the surface of a package to mount the element on a printed circuit board.

Furthermore, Japanese Patent Unexamined Publication No. 6-268101 discloses a semiconductor

device in which recesses for h using xternal t rminals are formed on a surfac of a packag .

According to the arts disclosed in Japanese Patent Unexamined Publication No. 6-224259, WO 92/05582 Publication, and Japanese Patent Unexamined Publication No. 6-302604 among the above prior arts, it is possible to obtain a semiconductor device having a plane size almost equal to the plane size of a semiconductor element. However, in any case, the structure of a semiconductor device is more complex than a conventional structure using a lead frame and moreover, it is necessary to develop an art which has not been used to connect electrodes of a semiconductor element with external terminals and form the external terminals. Therefore, the manufacturing cost of these semiconductor devices increases in general.

The arts disclosed in Japanese Patent Unexamined Publication No. 6-224259 and WO 92/05582 Publication have a problem that water easily enters the inside of a semiconductor device to deteriorate the moisture resistance of the semiconductor device because the whole surface of the semiconductor element is not covered with resin or the like and the semiconductor element is exposed from a package. Moreover, these prior arts have a problem that the arts cannot cope with the mass production of semiconductor devices because it is difficult to resin-seal a semiconductor elem nt by the transfer molding method frequently used for

conventional semiconductor devic s.

The semiconductor devices disclosed in Japanese Patent Unexamined Publication No. 6-224259, WO 92/05582 Publication, and Japanese Patent Unexamined Publication No. 6-132453 have a problem that a semiconductor device is warped because the electrode formed plane of a semiconductor element is covered with resin but the plane opposite to the electrode formed plane is exposed from a package and thereby, an uneven temperature distribution occurs in the inside of the device when a temperature change is applied.

The art disclosed in Japanese Patent Unexamined Publication No. 6-132453 has a problem that a defect (solder bridge defect) occurs in which leads arranged like a row are joined each other by solder when joining the leads with a printed circuit board by solder because a plurality of leads are arranged like a row on the surface of the package at short intervals. Moreover, because electrodes on the package surface are surface-mounted same as a conventional lead is, the strain at a solder joint due to the difference between the linear heat expansion coefficient of a package and that of a substrate increases and thermal fatigue breakdown easily occurs.

It is an object of the present invention to provide a CSP-type semiconductor device which can be mass-produced by the conventional semiconductor d vice manufacturing art such as the transfer molding method

and which has a high moisture resistance because a semiconductor element is completely sealed in a resin package, causes no solder bridge defect when the semiconductor device is mounted on a printed circuit board, and has a high resistance against thermal fatigue breakdown, and provide its manufacturing method.

Moreover, it is another object of the present invention to provide a semiconductor module having the above semiconductor devices.

DISCLOSURE OF THE INVENTION

A semiconductor device of the present invention comprises a semiconductor element having a plane with a plurality of electrodes formed on it, a plurality of internal leads electrically connected to said electrodes respectively, and an electrically insulating resin package for sealing said semiconductor element and said internal leads, in which said internal leads are substantially located in the range of said electrode formed plane, and said resin package has a plurality of external-terminal receiving recesses respectively reaching said internal leads in the range of said electrode formed plane.

In the case of a preferred embodiment, the external-terminal receiving recesses are formed by a resin plate having through-holes and integrally molded with said resin package.

Moreover, the resin plate can also have

recesses and film members forming th bott m of the r cesses and to be broken after integrally m lded with the resin package.

It is preferable that the external-terminal receiving recesses are tapered toward the internal leads.

It is preferable that the internal leads are bonded to the electrode formed plane by an electrically insulating adhesive.

It is possible to apply the electrically insulating adhesive only to a portion wherein the internal lead is electrically connected with the electrode and a portion where the internal lead is electrically connected with an external terminal.

It is preferable that the adhesive has an elastic modulus of 10 to 6,000 MPa. Moreover, it is preferable that the adhesive has a thickness of 20 to 100μm.

It is also possible that the internal leads protrude to the outside from the lateral of the resin package.

In the case of another embodiment, the semiconductor device further comprises a plurality of external terminals arranged in the external-terminal receiving recesses and electrically connected to the internal leads.

It is possible to use solder balls or conductive metals for the xternal terminals. When an

external terminal uses a solder ball, it is preferable that the solder ball has a height approx. two tim s larger than the depth of the external-terminal receiving recess.

The present invention moreover provides a method for manufacturing the above semiconductor device.

An embodiment of the semiconductor device manufacturing method comprises the steps of preparing a semiconductor element having a plane with a plurality of electrodes formed on it, preparing a multiple-string lead frame in which a plurality of internal leads are connected by an external frame, bonding said internal leads of the lead frame onto said electrode formed plane by an electrically insulating adhesive and electrically connecting said internal leads to said electrodes respectively, preparing a mold comprising an upper and an lower mold for defining a cavity for forming a resin package of which upper mold has protrusions for forming external-terminal receiving recesses, holding and securing said lead frame by said upper and lower molds while bringing said protrusions into contact with said internal leads, injecting resin into said cavity to seal said semiconductor element and internal leads, and separating said external frame from said internal leads at the lateral of said resin package.

An embodiment of the semiconductor device manufacturing method comprises the steps of preparing a semiconductor element having a plane with a plurality of

electrodes formed on it, preparing a multiple-string lead frame in which a plurality of int rnal l ads ar connected by an external frame, preparing a resin plate having through-holes for forming external-terminal receiving recesses, bonding said internal leads of said lead frame onto said electrode formed plane by an electrically insulating adhesive and thereafter bonding said resin plate onto said internal leads or bonding said resin plate onto said internal leads and thereafter bonding said internal leads onto said electrode formed plane by an electrically insulating adhesive, electrically connecting said internal leads to said electrodes respectively, preparing a mold comprising an upper and a lower mold for defining a cavity for forming a resin package, holding and securing said lead frame by said upper and lower molds while bringing the inside of said upper mold into contact with said resin plate, injecting resin into said cavity to seal said semiconductor element, said internal leads, and said resin plate, and separating said external frame from said internal leads at the lateral of said resin package.

An embodiment of the semiconductor device manufacturing method comprises the steps of preparing a semiconductor element having a plane with a plurality of electrodes formed on it, preparing a multiple-string lead frame in which a plurality of internal leads are conn ct d by an external fram , pr paring a resin plat having rec sses for forming xt rnal-terminal receiving

recesses and film members for forming the bottom of said recesses, bonding said internal leads of said lead frame onto said electrode formed plane by an electrically insulating adhesive and thereafter bonding said resin plate onto said internal leads or bonding said resin plate onto said internal leads and thereafter bonding said internal leads onto said electrode formed plane by an electrically insulating adhesive, electrically connecting said internal leads to said electrodes respectively, preparing a mold comprising an upper and a lower mold for defining a cavity for forming a resin package, holding and securing said lead frame by said upper and lower molds while bringing an inside surface of said upper mold into contact with said film members of said resin plate, injecting resin into said cavity to seal said semiconductor element, said internal leads, and said resin plate, forming external-terminal receiving recesses by breaking said film members, and separating said external frame from said internal lead at the lateral of said resin package.

An embodiment of the semiconductor device manufacturing method comprises the steps of preparing a semiconductor element having a plane with a plurality of electrodes formed on it, preparing a resin tape having a plurality of first through-holes and a plurality of foil leads formed so as to cover the first through-holes, preparing a multiple-string resin frame in which resin plates having a plurality of second through-holes are

connected to an external fram by a hanging member, bonding the foil leads of said resin tape with foil leads onto said electrode formed plane by an electrically insulating resin and thereafter bonding said resin plate onto said resin tape such that the second through-holes of said resin plate are aligned with the first through-holes of said resin tape or bonding said resin plate onto said resin tape such that the second through-holes of said resin plate are aligned with the first through-holes of said resin tape and thereafter bonding the foil leads of said resin tape with foil leads onto said electrode formed plane by an electrically insulating adhesive, electrically connecting said leads to said electrodes respectively, preparing a mold comprising an upper and a lower mold for defining a cavity for forming a resin package, holding and securing said hanging member by said upper and lower molds while bringing an inside surface of said upper mold into contact with said resin plate, injecting resin into said cavity to seal said semiconductor element, said foil leads, and said resin plate, and separating said resin plate from said hanging member at the lateral of said resin package.

In the above methods, it is also possible to further provide the step of forming external terminals electrically connected to said leads by extending the inside of said external-terminal receiving r cesses before or after said external-frame or hanging-member

s parating step.

A semiconductor d vic of the present invention can be mass-produced because a multiple-string lead frame or a multiple-string resin plate is used and thereby, the conventional transfer molding method can be applied. Moreover, because a semiconductor element is completely sealed in a resin package, it is possible to obtain a semiconductor device with a high moisture resistance. Furthermore, because external terminals used to mount on a circuit board are received by recesses provided on a resin package, it is possible to prevent a solder bridge defect from occurring. Furthermore, because an electrically insulating adhesive between an internal lead and the electrode formed plane of a semiconductor element absorbs thermal strain, it is possible to improve the durability against thermal breakdown.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a first embodiment of a CSP-type semiconductor device of the present invention, which is locally cut out for clarification purpose;

Figure 2 is a sectional view of the first embodiment of a CSP-type semiconductor device of the present invention;

Figures 3a to 3f are sectional views showing a manufacturing method for the first emb diment;

Figure 4 is a perspective view of a multiple-string lead frame usable for the first embodiment;

Figure 5 is a sectional view showing a first modification of the first embodiment;

Figure 6 is a sectional view showing a second modification of the first embodiment;

Figure 7 is a perspective view of a third modification of the first embodiment, which is locally cut out for clarification purpose;

Figure 8 is a sectional view of the third modification in Figure 7;

Figure 9 is a perspective view of a fourth modification of the first embodiment, which is locally cut out for clarification purpose;

Figure 10 is a sectional view of the fourth modification in Figure 9;

Figure 11 is a perspective view of a fifth modification of the first embodiment, which is locally cut out for clarification purpose;

Figure 12 is a sectional view of the fifth modification in Figure 11;

Figure 13 is a sectional view of a sixth modification of the first embodiment;

Figure 14 is a sectional view of a seventh modification of the first embodiment;

Figure 15 is a sectional view of a second embodiment of a CSP-type semiconductor device of the present invention;

Figure 16 is a bottom view of the second embodiment of a CSP-typ semiconductor device of th present invention, which is locally cut out for clarification purpose;

Figure 17 is a sectional view showing the second embodiment of a CSP-type semiconductor device of the present invention mounted on a circuit board;

Figures 18a to 18g are sectional views showing a manufacturing method for the second embodiment;

Figures 19a to 19g are sectional views showing another manufacturing method for the second embodiment;

Figure 20 is a sectional view of the first modification of the second embodiment having the same purpose as the sixth modification of the first embodiment shown in Figure 13;

Figure 21 is a sectional view of a second modification of the second embodiment;

Figure 22 is a sectional view of a third modification of the second embodiment;

Figure 23 is a sectional view of a fourth modification of the second embodiment;

Figure 24 is a sectional view of a fifth modification of the second embodiment;

Figure 25 is a sectional view of the fifth modification of the second embodiment shown in Figure 24, which is locally cut out for clarification purpose;

Figure 26 is a bottom view of a sixth modification of the second embodiment, which is locally

cut out for clarification purpose;

Figure 27 is a sectional view of a s venth modification of the second embodiment;

Figure 28 is a bottom view of the sixth modification of the second embodiment shown in Figure 27, which is locally cut out for clarification purpose;

Figure 29 is a sectional view of a eighth modification of the second embodiment, in which internal leads are made of an insulating film with foil leads;

Figure 30 is a bottom view of the eighth modification of the second embodiment shown in Figure 29, which is locally cut out for clarification purpose;

Figures 31a to 31g are sectional views showing a manufacturing method for the eighth modification of the second embodiment;

Figure 32 is a top view of a multiple-string resin plate used for the eighth modification of the second embodiment;

Figure 33 is a sectional view of a modified form of the eighth modification of the second embodiment;

Figure 34 is a bottom view of the modified form of the eighth modification of the second embodiment shown in Figure 33;

Figure 35 is a sectional view of another modified form of the eighth modification of the second embodiment;

Figure 36 is a perspective view of a

semiconductor devices mounting module on which CSP-type semiconductor devices of the pr sent invention are mounted; and

Figure 37 is a side view of the semiconductor device mounting module shown in Figure 36.

BEST MODE FOR CARRYING OUT THE INVENTION

A semiconductor device of the present invention is described below by referring to the accompanying drawings.

In Figures 1 and 2, the first embodiment of a semiconductor device of the present invention is shown. Electrodes 2 of a semiconductor element 1 are arranged like columns at the central portion of the circuit formed plane of the element. A plurality of metallic-plate internal leads 3 are bonded to the circuit formed plane 1a of the semiconductor element 1 by an electrically insulating adhesive 4 and the electrodes 2 of the semiconductor element 1 are electrically connected with the internal leads 3 by wires 5. Moreover, these members are sealed with a resin package 11. The internal leads 3 are cut at the lateral of the package 11. Spherical external terminals 6 are connected to planes opposite to the bonded planes of the internal lead 3 and exposed to the outside of the resin package 11 through recesses 17 formed on the package 11.

As shown in Figure 2, the external t rminals 6 are conn cted to electrodes 13 of a printed circuit

board 12.

By using solder as the material of the external terminal 6, it is possible to directly join the external terminal 6 with the internal lead 3 and the electrode 13 of the printed circuit board 12. It is practical that the internal lead 3 and the external terminal 6 are electrically connected each other one to one. It is preferable to use Pb/Sn-base eutectic solder (approx. 40% of Pb and approx. 60% of Sn) frequently used for mounting of surface-mounting semiconductor devices as the material of solder. In this case, it is preferable to previously apply surface treatment such as solder plating, nickeling, or tinning to the joint surface of the internal lead 3 with the external terminal 6 to improve the wettability of solder in order to raise the connecting strength.

In the case of the semiconductor device of this embodiment, because the external terminals 6 are located in a range of a plane of the semiconductor element 1, it is possible to provide a CSP-type semiconductor device by making the plane dimension of the semiconductor device approach the plane dimension of the semiconductor element 1. It is adequately possible by the present art to increase the thickness of the resin package 11 at the lateral of the semiconductor element 1 up to approx. 0.1 to 0.5 mm and moreover, increase the thickness of resin above the semiconductor element and under the internal lead up to approx. 0.15

to 0.2 mm. Therefore, it is possible to set the plane dimension of the package, that is, the plane dimension of the semiconductor device to a value obtained by adding 0.2 to 1.0 mm to the plane dimension of the semiconductor element 1. Moreover, when the sum of the thickness of the internal lead 3 and that of the adhesive 4 equals 0.3 mm, it is possible to set the package thickness to a value obtained by adding 0.6 to 0.7 mm to the thickness of the semiconductor element 1.

A TSOP is a thin semiconductor device with the highest density among the semiconductor devices practically used at present. For example, when mounting a memory element by 8 mm by 15 mm on the TSOP, a mounting area of 12 mm by 18 mm is necessary at the outer periphery of leads. In the case of this embodiment, a mounting area of 9 mm by 16 mm is enough. Therefore, by using this embodiment, it is possible to decrease the mounting area to at least 2/3 or less. Thus, the semiconductor device of this embodiment is particularly effective to mount a memory element for which very high density mounting is requested but which does not have a large number of external terminals.

In the case of this embodiment, it is preferable to make the height of the external terminal 6 made of solder larger than the depth of the recess 17. Moreover, it is practical that the height is approx. two times larger than the depth of the recess 17. If the height exceeds a value two times larger than the depth

of the recess 17, protrusion portion of the solder easily moves to right and left when it is fused, adjacent solder pieces contact each other, and solder bridge defects may frequently occur.

A first-embodiment manufacturing method is described below by referring to Figures 3a to 3f.

Figure 3a shows a sectional view of the semiconductor element 1 used for this embodiment. The electrodes 2 are formed in two rows at the center of a circuit formed plane 1a of the element.

Then, as shown in Figure 3b, the internal leads 3 are bonded to the element 1 by the adhesive 4. As shown in Figure 4, every internal lead 3 is connected to an external frame 5 to form an integrated lead frame 14. In this step, it is possible to bond the electrically insulating adhesive 4 to the element 1 and thereafter bond the internal leads 3 or previously bond the electrically insulating adhesive 4 to the internal leads 3 and thereafter bond the adhesive 4 to the semiconductor element 1. Then, the internal leads 3 are electrically connected with the electrodes 2 of the semiconductor element 1 by wires 5. These steps are completely the same as those of an LOC-type semiconductor device whose manufacturing art is already established.

Then, as shown in Figure 3c, an upper mold 16 having protrusions 30 and a lower mold 29 clamp the internal leads 3 with the protrusions 30 urged against

the int rnal leads 3 and resin is injected into a cavity 11' from a gat 31 of the upper mold 16. As a result, recesses 17 shown in Figure 3d are formed on a sealed resin package 11.

Thereafter, as shown in Figure 3e, external terminals 6 are connected to the internal leads 3 by mounting and heating solder balls. When forming the external terminal 6, it is preferable to improve the wettability of solder in order to increase the joining strength by using flux or heating the external terminals 6 in an inert gas or reducing gas. Finally, the internal leads 3 are cut at the package lateral to disconnect it from an external frame 15 and obtain the CSP-type semiconductor device shown in Figure 3f.

In the case of the above method, the external terminals 6 are formed and thereafter the internal leads 3 are cut at the package lateral. When it is unnecessary to form external terminals, however, it is possible to cut the internal leads 3 at the package lateral without forming the external terminals 6.

As shown in Figure 4, the lead frame 14 is the multiple-string type like a lead frame used for a normal resin-sealed semiconductor device. Therefore, it is possible to form a plurality of packages at the same time.

Moreover, though not illustrated, it is possible to use short int rnal leads for the internal leads 3 from the beginning so as to omit cutting of the

internal leads or they may be cut at the stag of Figure 3b.

As described above, because the CSP-type semiconductor device of this embodiment can be fabricated by the manufacturing method same as that of a conventional resin-sealed semiconductor device, it is possible to raise the reliability and lower the manufacturing cost.

In the case of the first embodiment above described, the electrically insulating adhesive 4 is applied to the whole surface of the internal lead 3. However, when using a double-coated adhesive tape obtained by applying an adhesive to both sides of an electrically insulating tape instead of the adhesive, it is also possible to divide the double-coated adhesive tape into pieces 4a and 4b and apply the pieces 4a and 4b only to a wire-bonding portion of the internal lead 3 and a portion to which the external terminal 6 is connected respectively. Because a double-coated adhesive tape easily absorbs water and moreover, it is easily peeled in a package, it is preferable to decrease the area of the tape from the viewpoint of reliability. The portions to which the pieces 4a and 4b of the double-coated adhesive tape are applied are pressed against the internal lead 3 for wire bonding and resin sealing. Therefore, it is always necessary to apply a doubl -coated adh sive tape to the portions.

In the cas of th above first embodiment,

solder balls are used as external terminals. However, as shown in Figur 6, it is also p ssible to use c pper as the material of the external terminals 6, connect the external terminals 6 to the internal leads 3 by solder 32, and connect the internal leads 3 to electrodes 13 of a printed circuit board 12 by solder 33. By constituting the external terminals as described above, it is possible to prevent the external terminals 6 from being crushed when mounting on a substrate. Though the solder 32 and solder 33 can use the same material, it is preferable that the melting point of the solder 32 to be connected to the internal leads 3 is higher than that of the solder 33 to be connected to the electrodes 13 so that the solder 32 to be connected to the internal leads 3 is not melted when connecting the internal leads 3 to the electrodes 13 of the printed circuit board 12.

As shown in Figures 7 and 8, it is also possible to use an electrically insulating film 21 provided with foil leads 20 instead of the metallic-plate internal leads 3. The electrically insulating film 21 with foil leads can be the film used for a TCP (tape carrier package)-type semiconductor device. By using the electrically insulating film 21 with foil leads, it is possible to fine internal wiring and increase the degree of freedom of the position of the external terminals 6 and moreover, decrease the thickness of packag .

Moreover, as shown in Figures 9 and 10, it is

possible to us thermocompression bonding for connection with th electrodes 2 of th semic nductor elem nt 1 by extending the foil leads 20. This joining method is the same as that used for a TCP-type semiconductor device. By constituting a package as described above, it is possible to decrease the thickness of package compared to the modification shown in Figure 7.

Then, a case in which the electrodes 2 of the semiconductor element 1 are arranged at the margin of an element is described below by referring to Figures 11 and 12.

The internal lead 3 is joined with each electrode 2 by thermocompression bonding so as to cover the electrode 2. The internal leads 3 are cut at the lateral of the package 11. The external terminals 6 are joined to the backs of the electrode joining planes of the internal leads 3.

Though the electrode 2 of the semiconductor element 1 is generally made of aluminum, it is impossible to join aluminum with solder. However, by using copper for the internal lead 3, it is possible to thermocompression-bond the internal lead 3 with aluminum and moreover join the internal lead 3 with solder. Therefore, it is possible to join both the electrode 2 and the external terminal 6 with the internal lead 3. Moreover, by gold-plating the joint surface of the internal lead 3 for the electrode 2 and solder-plating or tinning the joint surface of the internal lead 3 for

an external terminal, it is possibl to more securely join th internal lead 3.

Because this semiconductor device can also be fabricated by using the multiple-string lead frame shown in Figure 4, it is possible to improve the reliability and reduce the manufacturing cost.

Though the internal leads 3 are cut at the lateral of the package 11 in the case of the above-described semiconductor device, it is also possible to cut the internal leads 3 at a position where the internal leads 3 are slightly protruded from the package lateral as shown in Figure 13. Thus, it is also possible to inspect characteristics of the semiconductor device by applying probes 32a and 32b to protrusions 3' of the internal leads. Of course, it is possible to perform the characteristic inspection by applying the probes to the external terminals 6. However, when the external terminals 6 are solder, the solder may be deformed by performing the inspection. In the case of this embodiment, probes are used for electrical contact with the protrusions 3' of the internal leads. However, it is also possible to use a socket for holding the protrusion 3'. Moreover, it is possible to apply a burn-in screening inspection to a semiconductor device by using a probe or socket.

In the case of the above embodiment including the modifications, an external terminals ar set when a semiconductor device is fabricated. However, as shown

in Figur 14, it is also possible to form holes for external terminals when fabricating a semiconductor device and set the external terminals when mounting the semiconductor device on a substrate or form objects equivalent to the external terminals at the substrate side and mount the semiconductor device on the substrate.

Then, the second embodiment of a semiconductor device of the present invention is described below by referring to Figures 15 and 16.

Electrodes 2 of a semiconductor element 1 are arranged like a column at the center of a circuit formed plane 1a of the element 1.

A plurality of internal leads 3 are bonded onto the electrode formed plane 1a of the semiconductor element 1 by an insulating adhesive 4 and are electrically connected to the electrodes 2 of the element 1 by wires 5. A resin plate 8 with through-holes 9 formed therein is bonded to a plane 3b at the side opposite to a plane 3a bonded with the electrode formed plane 1a of each lead 3 through an adhesive 7. These members are sealed by a resin package 11 so that a plane 8a on which openings of the through-holes 9 are present is exposed to the surface of the package 11. The through-holes 9 form recesses 17 for receiving external terminals 6. Each lead 3 is cut at the lateral of the package 11. A metallic external terminal 6 serving as electrical connecti n m ans between the semiconductor element and

the outsid is connected to th plane 3b of each lead 3 through the recess 17. The external terminal 6 of this embodiment is a solder ball.

Though the semiconductor device shown in this embodiment forms the package 11 by sealing the semiconductor element 1, leads 3, adhesive 4, wires 5, and resin plate 8 with a sealing resin 10, a part of each lead 3 is exposed from the lateral 11a of the package 11. The external terminals 6 are located at the bottom 11b of the package, formed in a range of the electrode formed plane 1a of the semiconductor element 1, and arranged in two columns along the longitudinal direction of the package 11. Moreover, a part of the external terminal 6 is spherically protruded beyond the package 11 so as to be connected with a circuit board for mounting a semiconductor device.

It is preferable to give a taper on the recess 17 so that the diameter at the bottom 11b of the package becomes larger than that of the side contacting the lead 3. By giving a taper on the recess 17 as described above, a spherical solder can easily be inserted into the recess 17 and the external terminal 6 can easily be formed.

It is preferable to use solder (e.g. Pb-Sn eutectic solder) frequently used for the mounting of surface-mounting semiconductor devices as the material of the external terminal 6. In this cas , it is preferable to apply surface treatment such as solder

plating, Ni (nickel) plating, or Sn (tin) plating to th joint surfac of th 1 ad 3 with th xternal t rminal 6. Moreover, it is possible to apply surface treatment such as solder plating, Ni (nickel) plating, or Sn (tin) plating to the inside of the through-hole 9 of the resin plate 8.

For the adhesives 4 and 7, can be used an insulating material such as polyimide resin, epoxy resin, or silicone resin. Particularly, for the adhesive 4 for bonding the lead 3 to the semiconductor element 1 used is a material with an elastic modulus of 10 to 6,000 MPa. By setting the elastic modulus of the adhesive 4 in the above range, the shape of the adhesive is stabilized (no outflow of adhesive occurs) when bonding the lead 3 and a preferable adhesiveness is obtained. Moreover, by setting the thickness of the adhesive 4 to 20 to 100μm for practical use, it is possible to improve the durability of the joint between an external terminal and a circuit board against fatigue breakdown due to repetition of temperature change after mounting a semiconductor device on the circuit board. This is because an adhesive layer absorbs and moderates a thermal strain produced at a solder joint portion due to the difference between the linear heat expansion coefficient of the semiconductor device and that of the circuit board.

It is also possible to use a double-coated adh sive tape obtained by applying the above adhesive

material to the both sid s of a tape made of polyimide r sin or the like as the adhesive 4.

Moreover, the resin plate 8 is made of an electrically insulating material which is not wettable by solder. Specifically, a film member made of polyimide resin, epoxy resin, silicone resin, bismaleimidotriazine or the like is used. Though the thickness of the resin plate 8 is set to a value in which a wire is not exposed from the surface of a package, a plate of which thickness is in a range of approx. 50 to 150μm is used.

A thin wire made of Au (gold), Ag (silver), Cu (copper), or Al (aluminum) with a diameter of 10 to 30μm is used as the wires 5.

The lead 3 is made of an Fe-Ni alloy (iron-nickel alloy or Fe-42Ni) or a Cu (copper) alloy and its thickness is set to approx. 0.1 to 0.2 mm.

Epoxy resin to which, for example, a phenol-based curing agent, silicone rubber, and filler (fused quartz with the maximum grain diameter of approx. 70μm) are added is used as the sealing resin 10.

The semiconductor device shown in this embodiment is mounted on the circuit board 12 by making the side 11b of the external terminal formed plane (bottom) of the package 11 face the circuit board 12 as shown in Figure 17. The semiconductor device is electrically connected with the circuit board 12 by arranging each external terminal 6 on its corresponding

electrode 13 of the circuit board 12 and joining th ext rnal terminals 6 with th electrod s 13 of th circuit board. When the external terminals 6 are made of solder, they are joined with the electrodes 13 of the circuit board 12 by fusing the external terminals 6 after mounting the device on the circuit board 12. When the external terminals 6 are made of a material other than solder (e.g. Cu or Ni), they are joined by supplying solder to joint portions (by, for example, the printing method) and fusing the solder. To join the external terminals 6 with the electrodes 13 of the circuit board 12, it is preferable to improve the wettability of solder by, for example, using flux.

The thickness 6a of the external terminal 6 represents the distance from the contact portion with the lead 3 to the front end of the external terminal 6 in the direction perpendicular to the electrode formed plane 1a of the semiconductor element 1. It is preferable to set the thickness 6a of the external terminal to a value approx. two times larger than the depth 17a of the recess. By setting the thickness 6a to the value, it is possible to increase the height of the external terminal 6 when the external terminal 6 is made of solder. Thereby, it is possible to moderate thermal strain produced at the solder joint portions between the external terminals and the circuit board by deformation of the external t rminals themselves du to a temperature chang after th semiconductor device is

mounted on the circuit board and it is possible to increas the reliability of the solder joint portions.

According to the semiconductor device of this embodiment, it is possible to make the external size of a package approach the size of a semiconductor element because external terminals are located in the plane dimension (in the plane) of the electrode formed plane of the semiconductor element. When setting the resin thickness 10a (Figure 14) at the lateral of the semiconductor element 1 to 0.1 mm or more, the filler added in the resin 10 is smoothly injected into a mold at the time of resin sealing without clogging. By setting the resin thickness 10a to 0.1 ~ 0.5 mm, the semiconductor element 1 does not move from a predetermined position in the mold at the time of resin sealing and the semiconductor element and the wires are not exposed from the package.

Therefore, it is possible to obtain a package smaller than a dimension obtained by adding 1.0 mm to the plane dimension of a semiconductor element. Moreover, in the case of the semiconductor device of this embodiment, it is possible to improve the reliability of the moisture resistance or the like because the semiconductor element can be covered with resin similarly to the case of a conventional semiconductor device. Furthermore, because the semiconductor lem nt is almost uniformly covered with the s aling resin, it is possible to reduce the warpage of

the semiconductor device. Furthermore, because external terminals ar enclosed by a material to which solder is not wettable, it is difficult for a solder bridge defect to occur when mounting the semiconductor device on a circuit board.

A manufacturing method for the semiconductor device of the second embodiment is described below by referring to Figures 18a to 18g.

Figure 18a shows a sectional view of a semiconductor element 1 used for this embodiment. Electrodes 2 are formed at the center of the electrode formed plane 1a of the semiconductor element 1. Moreover, a not-illustrated protective film (passivation) for protecting the circuit of the semiconductor element 1 is formed on the electrode formed plane 1a of the semiconductor element 1 except at least the wire joint portions of the electrodes 2.

As shown in Figure 18b, leads 3 are bonded to the electrode formed plane 1a of the semiconductor element 1 by an insulating adhesive 4. A resin plate 8 provided with through-holes 9 serving as recesses for receiving external terminals after forming a package is bonded to sides 3b opposite to the bonding planes of the leads 3 with the semiconductor element 1 by an adhesive 7. The leads 3 are connected to an external frame 15 to form a integrated lead frame 14 as shown in Figure 4.

In th st p of Figure 20b, it is also possible to bond the l ad frame 14 in which the adhesive 4 and

resin plat 8 are bonded to th leads 3 onto the semiconductor element 1 or separately bond the adh sive 4, lead frame 14, and resin plate 8 onto the semiconductor element 1.

Then, as shown in Figure 18c, the leads 3 and the electrodes 2 of the semiconductor element 1 are electrically connected each other by wires 5. The above steps are completely the same as those of an LOC (Lead On Chip)-type semiconductor device whose manufacturing art is already established.

Then, as shown in Figure 18d, the thus formed semiconductor element 1 is set in a mold 16, 29 of the transfer-molding to seal them with resin. In this case, molding is performed while bringing a plane 8a of the resin plate 8 into contact with an inside surface 16a of an upper mold 16. By bringing the plane 8a of the resin plate 8 into contact with the upper mold 16, it is possible to prevent the resin from entering the through-holes 9 from the circumference of the plane 8a of the resin plate 8. Moreover, it is preferable to set the thickness of the resin plate 8 to a value larger than the dent value A of the upper mold 16 at the side with which the plane 8a of the resin plate 8 contacts. By setting the thickness to the value, it is possible to increase the contact force between the resin plate 8 and the upper mold 16. Furthermore, the external frame 15 of th lead frame 14 is held by the upper mold 16 and lower mold 29 so that the semiconductor element 1 r the

like is not moved due to th inflow pressure of the resin in the upper mold 16 and lower mold 29.

After resin sealing, the plane 8a of the resin plate 8 is exposed and the recesses 17 for housing external terminals are formed on the surface of the package 11 as shown in Figure 18e. Thereafter, as shown in Figure 18f, the external terminals 6 are joined with the leads 3 by setting solder balls serving as the external terminals 6 in the recesses 17 and heating the balls. When joining the solder balls, it is preferable to improve the wettability of solder by using flux or heating the solder balls in an inert gas or a reducing gas. Finally, as shown in Figure 18g, the external frame 15 of the lead frame 14 is cut at the package lateral 11a to obtain the semiconductor device shown in Figures 14 and 15.

In the case of the above method, the external terminals 6 are formed and thereafter, the internal leads 3 are cut at the package lateral. Unless any external terminal is necessary, however, it is possible to cut the internal leads 3 at the package lateral without forming the external terminals 6.

The lead frame used for this embodiment shown in Figure 4 is the multiple-string type in which a plurality of same parts are connected each other and a plurality of packages can be formed by one-time molding.

Another manufacturing meth d for the second embodim nt is describ d below by referring to Figures

19a to 19g.

Figure 19a shows a sectional view of th semiconductor element 1 used for this embodiment. Electrodes 2 are formed at the center of the electrode formed plane 1a of the semiconductor element 1. Moreover, a not-illustrated protective film (passivation) for protecting the circuit of the semiconductor element 1 is formed on the electrode formed plane 1a of the semiconductor element 1 except at least the wire joint portions of the electrodes 2.

As shown in Figure 19b, leads 3 are bonded to the electrode formed plane 1a of the semiconductor element 1 through an insulating adhesive 4. A resin plate 8 provided with recesses 18 serving as portions for receiving external terminals after forming a package is bonded to a plane 3b opposite to the bonding plane of the lead 3 with the semiconductor element 1 by the adhesive 7. The recesses 18 open at the bonding plane side of the resin plate 8 with the leads 3 and film members 19 are provided at the side opposite to the bonding plane side. The film members 19 are made of the same material as that of the resin plate 8. The leads 3 are connected to the external frame 15 as shown in Figure 4 to form the integrated lead frame 14. In the step of Figure 19b, it is possible to bond the lead frame 14 in which the adhesive 4 and resin plate 8 are bonded to the leads 3 nto the semiconductor element 1 or separately b nd the adhesive 4, lead frame 14, and

resin plate 8 onto th semiconductor element 1.

Then, as shown in Figure 19c, the leads 3 and the electrodes 2 of the semiconductor element 1 are electrically connected each other by wires 5.

Then, as shown in Figure 19d, the thus formed semiconductor element is set in the mold 16, 29 of transfer-molding to seal them with resin. In this case, molding is performed while pressing the plane 8a of the resin plate 8 at the film member side against the inside surface 16a of the upper mold 16. The film members 19 of the recesses 18 prevent resin from entering the recesses 18. Moreover, the external frame 15 of the lead frame 14 is held by the upper mold 16 and lower mold 29 so that the semiconductor element 1 or the like is not moved due to the inflow pressure of resin in the upper mold 16 and lower mold 29.

After resin sealing, as shown in Figure 19e, the plane 8a of the resin plate 8 at the film member side is exposed. After resin sealing, as shown in Figure 19e, the film members 19 are broken by, for example, a needle-shaped member 28 to remove the members 19 and form recesses 17 for receiving external terminals on the surface of the package 11. Thereafter, as shown in Figure 19f, the external terminals 6 are joined to the leads 3 by setting solder balls serving as the external terminals 6 in the recesses 17 and heating the balls. Finally, as shown in Figure 19g, the external frame 15 of th lead fram 14 is cut at the package

lateral 11a to obtain the semiconductor device shown in Figures 15 and 16.

In the case of the above method, the external terminals 6 are formed and thereafter, the lead frame 14 is cut at the package lateral. However, unless any external terminal is necessary, it is possible to cut the lead frame 14 at the package lateral without forming the external terminals 6.

It is possible to form the film member 19 with the material same as that of the resin plate 8 or a material different from that of the resin plate 8. Moreover, it is possible to remove the film member 19 after resin sealing by etching according to chemicals or fuse and remove the member 19 by forming it with a material having a melting point lower than that of the resin plate 8 or sealing resin 10.

Figure 20 shows another modification of the second embodiment. A part of leads 3 are exposed to the outside from the lateral 11a of the package 11 to form protrusions 3c. Similarly to the modification of the first embodiment shown in Figure 13, the protrusions 3c of the leads can be used as terminals for inspecting operations of the semiconductor element 1. Even after the semiconductor device is mounted on a circuit board, the semiconductor device can be inspected by bringing an inspection probe into contact with the protrusions 3c.

Figure 21 shows a s cond modification of the second embodiment. A part of the leads 3 are exposed to

the outside from th lat ral 11a of th package 11 and extended and joined with th circuit board 12 as radiating leads 3d by solder or the like. By joining a part of the leads 3 with the circuit board as radiating leads, it is possible to decrease the heat resistance of the package and improve the heat radiating characteristic of the semiconductor device. Moreover, the radiating leads 3d are not only bonded with the circuit board 12 as shown in Figure 21 but also it is possible to form the leads 3 into a structure for radiating heat in the space around the semiconductor device by folding them in the direction opposite to the circuit board 12.

Moreover, in the case of the second embodiment shown in Figures 15 and 16, the length of the adhesive 4 for bonding the lead 3 to the electrode formed plane 1a of the semiconductor element 1 is set to a value almost equal to the lead 3 present on the electrode formed plane 1a. However, it is not necessary to set the adhesive 4 in an excessive wide range only if the lead 3 is secured to the electrode formed plane 1a of the semiconductor element 1. Therefore, it is only necessary to set the adhesive 4 only to the joint portion of the lead 3 with the wire 5 as shown in Figure 22. By decreasing the applying range of the adhesive 4, it is possible to decrease a stress produced in the package due to heating when mounting the semiconductor device on the circuit board (caused by a high pressure produced when water absorbed by the adh sive is

vaporated). Thereby, it is possible to prevent a defect such as interface separation in a package or resin crack from occurring.

The external terminals 6 are used to join a semiconductor device with an external object (e.g. circuit board) and form electrical connections. Therefore, it is enough that the external terminals 6 are supplied to the recesses 17 of the package 11 or joint portions of the circuit board to be connected to the external terminals when mounting the semiconductor device on the circuit board. Therefore, it is possible that a semiconductor device has not only the structure provided with the external terminals 6 like the second embodiment shown in Figures 15 and 16 but also a structure provided with no external terminal. Figure 23 shows a semiconductor device of the present invention provided with no external terminal. In the case of the semiconductor device, the recesses 17 for housing external terminals are formed on the surface of the package 11 and solder is supplied to the recesses 17 when mounting the semiconductor device on a circuit board to form the external terminals 6 for connecting the semiconductor device with the circuit board. The semiconductor device mounted on the circuit board shown in Figure 23 is the same as that shown in Figure 17.

The second embodiment shown in Figures 15 and 16 shows the semiconductor device in which the electrodes 2 of the semiconductor element 1 are arranged

like a column at the central portion of the lectrode formed plane 1a. However, Figures 24 to 28 show a semiconductor device in which electrodes 2 are arranged around an electrode formed plane 1a.

In Figures 24 and 25, the electrodes 2 of the semiconductor element 1 are formed at the long-side ends of the semiconductor element 1 and joined with leads 3 extending to the central portion of the semiconductor element 1 from the long side of it by wires 5. Moreover, the leads 3 are arranged at positions not covering the electrodes 2 arranged around the electrode formed plane 1a. The example shown in Figures 24 and 25 is the same as the second embodiment shown in Figures 15 and 16 except the forming place of the electrodes 2 and the joint places of the electrodes 2 and leads 3.

Figure 26 shows a semiconductor device in which the electrodes 2 of a semiconductor element 1 are arranged around an electrode formed plane 1a.

The electrodes 2 of the semiconductor element 1 are formed at the long-side ends of the semiconductor element 1 and joined with leads 3 extended up to the vicinity of the electrodes 2 to be connected from the short side of the semiconductor element 1 by wires 5.

In Figures 27 and 28, electrodes 2 are arranged on a periphery portion of an electrode formed plane 1a of the semiconductor element 1 and leads 3 are dir ctly joined with the electrodes 2. Metallic ext rnal terminals 6 serving as electrical connection

means between the semiconductor element and an external bject are connected to planes 3b f the leads pposit to joint planes 3a with the electrodes 2. The external terminals 6 are coaxially located with the electrodes 2 of the semiconductor element 1 and their positions on the plane coincide with each other. A resin plate 8 having through-holes 9 is bonded to the surface 3b of the leads 3, openings of the through-holes 9 of the resin plate 8 are exposed to the surface of a package, and recesses 17 for receiving the external terminals 6 are formed on the surface of the package.

It is preferable to use solder (e.g. Pb-Sn-based eutectic solder) frequently used for surface-mounting semiconductor devices as the material of the external terminals 6. In this case, it is preferable to apply surface treatment such as solder plating, Ni (nickel) plating, or Sn (tin) plating to the joint portions of the leads 3 with the external terminals 6.

The leads 3 used for this embodiment are made of a Cu (copper) alloy and their thickness ranges from approx. 0.05 to 0.2 mm.

The electrodes 2 of the semiconductor element 1 are generally made of Al (aluminum) and the electrodes 2 can directly be joined with the leads 3 by using Cu for leads 24. Moreover, the electrodes 2 can securely be joined with the leads 3 by applying surface treatment such as Au (gold) plating to the joint portions f the lead 3 with the electrodes 2.

As shown in Figures 29 and 30, it is p ssible that a resin tape 21 with foil l ads 20 formed on it is bonded to the electrode formed plane 1a of the semiconductor element 1 instead of the metallic-plate leads 3 by an adhesive 4. One end 20a of the foil lead 20 and the electrode 2 are electrically connected with each other by thermocompression bonding or the like. A plurality of through-holes 22 are formed on the resin tape 21. One end 20b of the foil lead 20 is extended so as to cover an opening 22a of the through-hole 22 at the electrode formed plane side.

A resin plate 8 having a plurality of through-holes 9 is bonded to a plane 21b opposite to the plane 21a of the resin tape 21 bonded with the electrode formed plane 1a by an adhesive 7 and the through-holes 9 of the resin plate 8 and the through-holes 22 of the resin tape 21 are aligned with each other. In the case of this embodiment, the recesses 17 for housing the external terminals 6 are formed on the surface of the package by bonding the resin plate 8 provided with the through-holes 9 to the resin tape 21 and exposing a plane 8a of the resin plate 8 to the surface of the package 11. Metallic external terminals 6 serving as electrical connection means between the semiconductor device and an external object are housed in the recesses 17 (comprising the through-holes 22 of the resin tape 21 and th through-holes 9 of the resin plat 8) and joined with the nds 20b of the foil leads 20.

In the cas of the semiconductor device, the package 11 is formed by sealing the semiconductor element 1, resin tape 21, adhesive 4, foil leads 20, and resin plate 8 with the sealing resin 10. The external terminals 6 are located at the bottom 11b of the package and formed in a range of the electrode formed plane 1a of the semiconductor element 1 and arranged like an array. Moreover, a part of each of the external terminals 6 is spherically protruded to the outside of the package 11 so that it can be connected with a circuit board for mounting the semiconductor device. Hanging members 23a extending to four corners of the package 11 from the resin plate 8 are formed on the bottom 11b of the package where the plane 8a of the resin plate 8 is exposed. The hanging members 23a are used to secure the package constituting members such as the semiconductor element 1 in a mold at the time of resin sealing.

As the resin tape 21 with the foil leads 20, a tape carrier used for a conventional tape carrier package (TCP) is used. The foil leads 20 can be joined with the electrodes 2 of the semiconductor element 1 by the tape automated bonding (TAB) art. The foil leads 20 are made of Cu (copper) or Au (gold) and the resin tape 21 is made of polyimide resin or the like.

It is preferable to use solder (e.g. Pb-Sn-based eutectic sold r) frequently us d for surface-m unting semiconductor d vices as the mat rial of the

external terminals 6. In this case, it is preferable to apply solder plating, Ni (nickel) plating, or Sn (tin) plating to the joint portions of the foil leads 20 with the external terminals 6.

As the adhesives 4 and 7, an insulating material such as polyimide resin, epoxy resin, or silicone resin is used. Particularly, for the adhesive 4 for bonding the resin tape 21 to the semiconductor element 1, a material with an elastic modulus of 10 to 6,000 MPa is used. By setting the elastic modulus of the adhesive 4 in the above range, the shape of the adhesive is stabilized when bonding the resin tape 21 and a preferable adhesiveness is obtained, and moreover it is possible to improve the durability of the solder joint portions between the external terminals and the circuit board against fatigue breakdown due to repetition of temperature change after mounting the semiconductor device on the circuit board.

According to the present semiconductor device, it is possible to make the plane size of a package approach the plane size of a semiconductor element because external terminals are located in the plane dimension (in the plane) of the electrode formed plane of the semiconductor element. By setting the resin thickness 10a around the semiconductor element 1 to 0.1 mm or more, filler added in the resin 10 is smoothly injected into a mold at the time of resin sealing without clogging.

Moreover, by setting the resin thickness 10a at approx. 0.5 mm, the semiconductor element 1 does not move from a predetermined position upon molding. Therefore, it is possible to obtain a package with a dimension obtained by adding 1.0 mm to the plane dimension of the semiconductor element or less. Moreover, the present semiconductor device can be covered with resin similarly to the case of a conventional semiconductor device, it is possible to improve the reliability of the moisture resistance or the like. Furthermore, because the external terminals 6 can be arranged like an array at the bottom of a package, it is possible to cope with increase of the number of terminals (increase of the number of pins) of a semiconductor device.

In the case of the modification of the second embodiment shown in Figures 29 and 30, a case is shown in which the external terminals 6 are arranged like an array at the bottom of the package. However, the arrangement of the external terminals 6 is not restricted to the array shape. It is also possible to use the two-column arrangement shown in Figures 15 and 16 or the arrangement of one column or the arrangement of three columns or more.

Then, a manufacturing method for the modification of the second embodiment shown in Figures 29 and 30 is described below by referring to Figures 31a to 31g.

Figure 31a shows a sectional view of the

semiconductor element 1 used for this embodim nt. The electrodes 2 are formed on a periphery portion of th electrode formed plane 1a of the semiconductor element 1. Moreover, a not-illustrated protective film (passivation) for protecting the circuit of the semiconductor element 1 is formed on the electrode formed plane 1a of the semiconductor element 1 except at least the foil lead joint portion of the electrodes 2.

As shown in Figure 31b, the resin tape 21 with foil leads 20 is bonded to the electrode formed plane 1a of the semiconductor element 1 by the insulating adhesive 4 so that the foil lead formed plane 21a faces the electrode formed plane 1a. The resin tape 21 is provided with through-holes 22 for joining external terminals with the foil leads 20. The resin plate 8 provided with through-holes 9 serving as recesses for housing the external terminals after forming a package is bonded to the plane 21b opposite to the plane of the resin tape 21 bonded with the semiconductor element 1 by the adhesive 7 so that the through-holes 22 of the resin tape 21 align with the through-holes 9 of the resin plate 8. The resin plate 8 is connected to the external frame 23b shown in Figure 32 by hanging members 23a to form a frame-shaped member 23 in which a plurality of same parts are connected.

In the step of Figure 31b, it is also possible t bond the resin plate 8 on which the adhesive 4 is applied and the resin tape 21 is bonded by the adhesive

7 onto the semiconductor elem nt 1 by the adhesive 4 or bond the resin tape 21 to th semiconductor lem nt 1 by the adhesive 4 and thereafter bond the resin plate 8 onto the resin tape 21 by the adhesive 7.

Then, as shown in Figure 31c, the foil leads 20 and the electrodes 2 of the semiconductor element 1 are joined each other by thermocompression bonding or the like. It is possible to join the foil lead 20 with the electrode 2 of the semiconductor element 1 by the conventional TAB art.

Then, as shown in Figure 31d, the thus formed assembly is set in a mold 16, 29 of the transfer-molding to seal with resin. In this case, molding is performed by bringing the outside plane 8a of the resin plate 8 into contact with the inside surface 16a of an upper mold 16. By bringing the plane 8a of the resin plate 8 into contact with the upper mold 16, it is possible to prevent resin from entering the through-holes 9 from the circumference of the plane 8a of the resin plate 8. Moreover, parts of hanging members 23a are held by the upper mold 16 and lower mold 29 so that the semiconductor element 1 or the like is not moved due to the inflow pressure of resin in the upper mold 16 and lower mold 29.

After resin sealing, the outside plane 8a of the resin plate 8 is exposed and recesses 17 for receiving external terminals ar formed on the surface of the package 11 as shown in Figure 31e. Th reafter,

as shown in Figure 31f, th ext rnal terminals 6 are joined to the foil leads 20 by mounting solder balls serving as the external terminals 6 in the recesses 17 and heating them. For joining of the solder balls, it is preferable to improve the wettability of solder by using flux or heating the balls in an inert gas or an reducing gas. Finally, as shown in Figure 31g, the hanging members 23a are cut at the lateral of the package to obtain the semiconductor device shown in Figures 29 and 30.

In the above method, the external terminals 6 are formed and thereafter, the hanging members 23a are cut at the lateral of the package. However, unless any external terminal is necessary, it is possible to cut the hanging members 23a at the lateral of the package without forming the external terminals 6.

The modification of the second embodiment of the semiconductor device of the present invention shown in Figures 29 and 30 uses the resin film with foil leads. However, it is possible to omit the resin film if desired as shown in Figure 33. In Figure 33, the foil leads 20 are bonded to the formed plane 1a of the electrode 2 of the semiconductor element 1 by the adhesive 4 and ends 20a of the foil leads 20 and the electrodes 2 are joined by thermocompression bonding. The foil leads 20 are directly bonded to the resin plate 8 by the resin 7.

In th case of the embodiment shown in Figures

33 and 34, th foil leads 20 are directly b nded to the resin plate 8 by th adh sive 7. However, it is also possible to use a structure using no adhesive 7 by forming the foil leads 20 on the resin plate 8 through the plating method or vacuum evaporation method as shown in Figure 35. In the case of the structure shown in Figure 35, it is possible to use a conventional tape material for a TCP and use the conventional semiconductor device manufacturing art.

Figures 36 and 37 show a semiconductor module in which semiconductor devices 26 of the present invention are mounted on a circuit board 12. Moreover, the circuit board 12 is provided with a socket for connection with an external unit. The semiconductor devices 26 are mounted on the surface 12a of the circuit board 12 by the external terminals 6 provided in the bottom 11b of the package facing the surface 12a of the circuit board 12 (plane at the side facing the circuit board 12).

The semiconductor module shown in Figures 36 and 37 has the semiconductor devices 26 including semiconductor elements mainly operating as memory and it is used as a memory card or memory module.

According to the semiconductor module shown in Figures 36 and 37, because external terminals are provided in an area of the bottom of the semiconductor device, it is possible to decrease the intervals among adjacent semiconductor devices, mount more semiconductor

devices on a circuit board which is the same size as an conventional circuit board, and r alize a high mounting density. Or, if a semiconductor module of the invention has functions equivalent to conventional ones, it can be more compact. Moreover, in the case of a semiconductor device of the present invention, a portion between external terminals is made of a material for preventing solder from wetting. Therefore, no defect (solder bridge defect) in which solder is joined between a plurality of external terminals occurs when mounting the semiconductor device and a semiconductor module improving the mounting yield is obtained. Furthermore, because a solder joint portion is not covered with resin differently from the bare chip mounting, it is possible to easily replace a semiconductor device having a defect with a new one.

CLAIMS:

1. A semiconductor d vic comprising:

a semiconductor element (1) having a plane (1a) with a plurality of electrodes (2) formed thereon;

a plurality of internal leads (3; 20) electrically connected to said electrodes (2) respectively; and

an electrically insulating resin package (11) for sealing said semiconductor element (1) and said internal leads (3; 20); characterized in that

said internal leads (3; 20) are substantially located in the range of said electrode formed plane (1a) and said resin package (11) has a plurality of external terminal receiving recesses (17) respectively reaching said internal leads (3; 20) in the range of said electrode formed plane (1a).

2. The semiconductor device according to claim 1, wherein said external terminal receiving recesses (17) is formed by a resin plate (8) having through-holes (9) and integrally molded with said resin package (11).

3. The semiconductor device according to claim 2, wherein said resin plate (8) has recesses (18) and film members (19) forming the bottom of said recesses (18) and to be broken after integrally molded with said resin package (11).

4. The semiconductor device according to claim 1, 2, r 3, wherein said external terminal receiving recesses (17) are tapered toward said internal leads (3;

20).

5. The semiconductor device according to claim 1, 2, or 3, wherein said external terminal receiving recesses (17) are arranged like at least one column.

6. The semiconductor device according to claim 1, 2, or 3, wherein said external terminal receiving recesses (17) are arranged like an array.

7. The semiconductor device according to claim 1, wherein said internal leads (3) are metallic plate leads, mounted on said electrodes (2), and compression-bonded to said electrodes.

8. The semiconductor device according to claim 1, wherein said internal leads (3; 20) are electrically connected to said electrodes (2) by wires (5).

9. The semiconductor device according to claim 1, wherein said internal leads (3; 20) are electrically connected to said electrodes (2) by thermocompression bonding.

10. The semiconductor device according to claim 1, wherein said internal leads (3; 20) are bonded to said electrode formed plane (1a) by an electrically insulating adhesive (4).

11. The semiconductor device according to claim 10, wherein said electrically insulating adhesive (4) is arranged at portions of said internal leads (3) used for electrical connection with said electrodes (2) and at portions of said internal leads (3) used for electrical connection with external terminals (6).

12. The semiconductor device according to claim 10, wherein said electrically insulating adhesive (4) is arranged at portions of said internal leads (3) used for electrical connection with said electrodes (2).

13. The semiconductor device according to claim 10, 11, or 12, wherein said adhesive (4) has an elastic modulus of 10 to 6,000 MPa.

14. The semiconductor device according to claim 10, 11, or 12, wherein said adhesive (4) has a thickness of 20 to 100μm.

15. The semiconductor device according to claim 1, wherein said internal leads (3) protrude outward from the lateral of said resin package (11).

16. The semiconductor device according to claim 1, wherein said semiconductor device further comprises a plurality of external terminals (6) arranged in said external terminal receiving recesses (17) and electrically connected to said internal leads (3; 20) respectively.

17. The semiconductor device according to claim 16, wherein said external terminals (6) are solder balls.

18. The semiconductor device according to claim 16, wherein said external terminals (6) are made of conductive metal.

19. The semiconductor device according to claim 17, wherein said solder balls (6) have a height about two times larger than the depth of said external

terminal receiving recess s (17).

20. A method for manufacturing the semiconductor device of claim 1, comprising the steps of:

preparing a semiconductor element (1) having a plane (1a)with a plurality of electrodes (2) formed thereon;

preparing a multiple-string lead frame (14) in which a plurality of internal leads (3) are connected by an external frame (15);

bonding said internal leads (3) of said lead frame (14) onto said electrode formed plane (1a) by an electrically insulating adhesive (4) and electrically connecting said internal leads (3) to said electrodes respectively;

preparing a mold comprising an upper mold (16) and a lower mold (29) for defining a cavity (11') for forming a resin package (11), said upper mold (16) having protrusions (30) for forming external terminal receiving recesses (17);

holding and securing said lead frame (14) by said upper mold (16) and lower mold (29) while bringing said protrusions (30) into contact with said lead frame (14) and injecting resin into said cavity (11') to seal said semiconductor element (1) and internal leads (3); and

separating said external frame (15) from said int rnal leads (3) at the lateral of said resin package (11).

21. A method for manufacturing the semiconductor device of claim 2, comprising the steps of:

preparing a semiconductor element (1) having a plane (1a) with a plurality of electrodes (2) formed thereon;

preparing a multiple-string lead frame (14) in which a plurality of internal leads (3) are connected by an external frame (15);

preparing a resin plate (8) having through-holes (9) for forming external terminal receiving recesses (17);

bonding said internal leads (3) of said lead frame (14) onto said electrode formed plane (1a) by an electrically insulating adhesive (4) and thereafter bonding said resin plate (8) onto said internal leads (3) or bonding said resin plate (8) onto said internal leads (3) and thereafter bonding said internal leads (3) onto said electrode formed plane (1a) by said electrically insulating resin (4);

electrically connecting said internal leads (3) to said electrodes (2) respectively;

preparing a mold comprising an upper mold (16) and a lower mold (29) for defining a cavity (11') for forming a resin package (11);

holding and securing said lead frame (14) by said upper mold (16) and lower mold (29) while bringing an inside (16a) surface of said upper mold (16) int contact with said resin plate (8) and injecting resin

into said cavity (11') to seal said internal leads (3) and said resin plate (8); and

separating said external frame (15) from said internal leads (3) at the lateral of said resin package (11).

22. A method for fabricating the semiconductor device of claim 3, comprising the steps of:

preparing a semiconductor element (1) having a plane (1a) with a plurality of electrodes (2) formed thereon;

preparing a multiple-string lead frame (14) in which a plurality of internal leads (3) are connected by an external frame (15);

preparing a resin plate (8) having recesses (18) for forming external terminal receiving recesses (17) and film members (19) for forming the bottom of said recesses (18);

bonding said internal leads (3) of said lead frame (14) onto said electrode formed plane (1a) by an electrically insulating adhesive (4) and thereafter bonding said resin plate (8) onto said internal leads (3) or bonding said resin plate (8) onto said internal leads (3) and thereafter bonding said internal leads (3) onto said electrode formed plane (1a) by said electrically insulating adhesive (4);

electrically connecting said internal leads (3) to said el ctrodes respectiv ly,

preparing a mold comprising an upp r mold (16)

and a lower mold (29) for d fining a cavity (11') for forming a resin package (11);

holding and securing said lead frame (14) by said upper mold (16) and lower mold (29) while bringing an inside surface (16a) of said upper mold (16) into contact with said film members (19) of said resin plate (8) and injecting resin into said cavity (11') to seal said semiconductor element (1), said internal leads (3), and said resin plate (8);

forming external terminal receiving recesses (17) by breaking said film members (19); and

separating said external frame (15) from said internal leads (3) at the lateral of said resin package (11).

23. The semiconductor device manufacturing method according to claim 20, 21, or 22, wherein said method further includes the step of forming external terminals (6) extending the inside of said external terminal receiving recesses (17) and electrically connected to said internal leads (3) before or after the step of separating said external frame (15).

24. A method for manufacturing the semiconductor device of claim 2, comprising the steps of:

preparing a semiconductor element (1) having a plane (1a) with a plurality of electrodes (2) formed thereon;

preparing a resin tape (21) having a plurality of first through-holes (22) and a plurality of foil

leads (20) formed so as to cover said first through-holes (22);

preparing a multiple-string resin frame in which a resin plate (8) having a plurality of second through-holes (9) is connected to an external frame (23) by hanging members (23a);

bonding the foil lead (20) of said resin tape (21) with foil leads onto said electrode formed plane (1a) by an electrically insulating adhesive (4) and thereafter aligning said second through-holes (9) of said resin plate (8) with said first through-holes (22) of said resin tape (21) to bond said resin plate (8) onto said resin tape (21) or aligning said second through-holes (9) of said resin plate (8) to said first through-holes (22) of said resin tape (21) to bond said resin plate (8) onto said resin tape (21) and thereafter bonding the foil leads (2) of said resin tape (21) with foil leads onto said electrode formed plane (1a) by said electrically insulating adhesive (4);

electrically connecting said foil leads (20) to said electrodes (2) respectively;

preparing a mold comprising an upper mold (16) and a lower mold (29) for defining a cavity (11') for forming a resin package (11);

holding and securing said hanging members (23a) by said upper mold (16) and lower mold (29) while bringing an inside surface (16a) of said upper mold (16) into contact with said resin plate (8) and injecting

resin into said cavity (11') to s al said semiconductor lement (1), said foil leads (20), and said r sin plat (8); and

separating said resin plate (8) from said hanging members (23a) at the lateral of said resin package (11).

25. The semiconductor device manufacturing method according to claim 24, wherein said method further includes the step of forming external terminals (6) extending said external terminal receiving recesses (17) and electrically connected to said foil leads (20) by before or after the step of separating said hanging members (23a).

26. A semiconductor module comprising a circuit board (12) having a socket (27) for connection with an external unit and a plurality of semiconductor devices of any one of claims 1 to 19 mounted on said circuit board (12).

FIG. 1

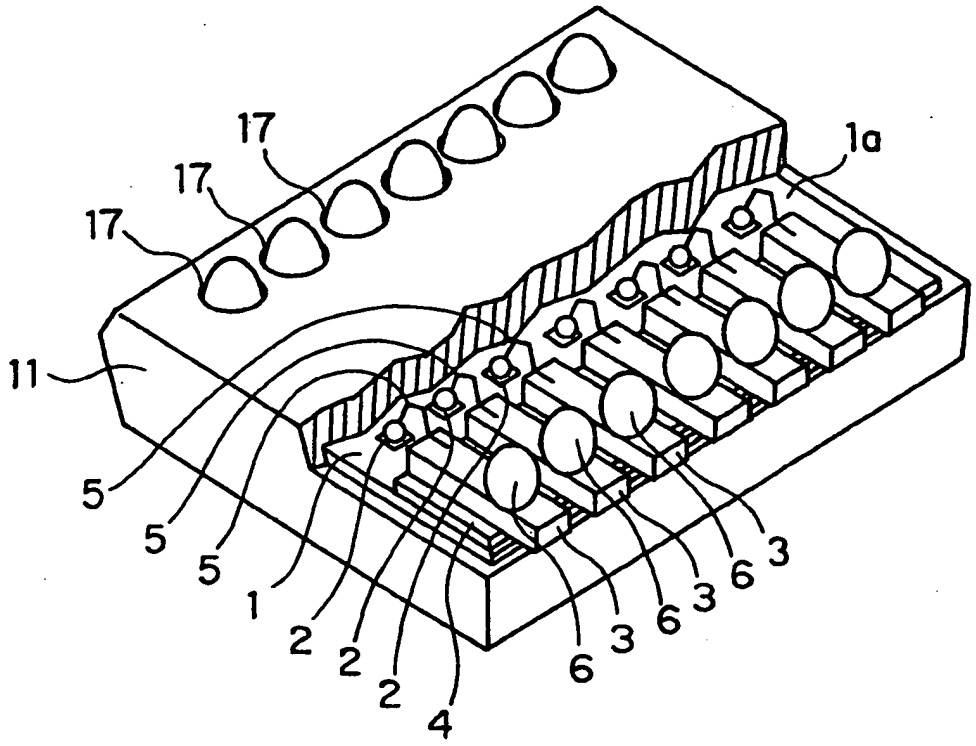


FIG. 2

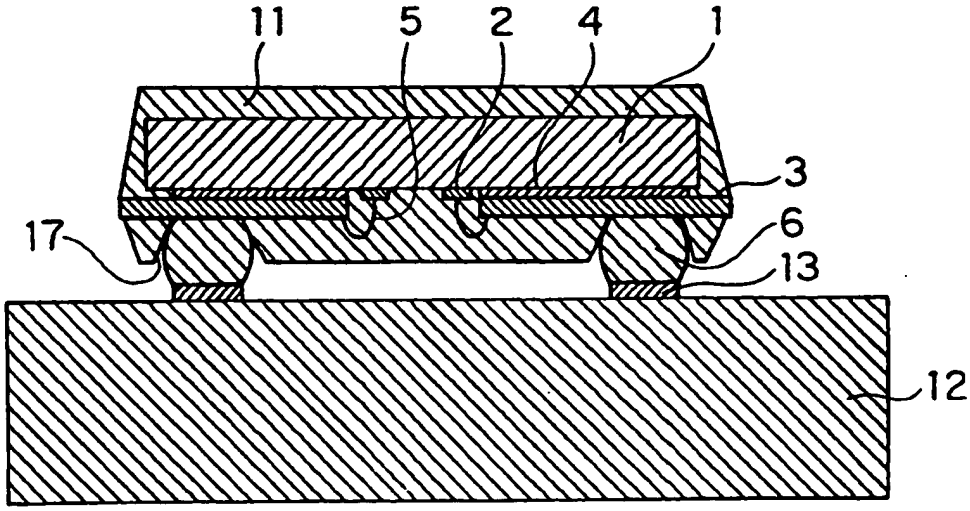


FIG. 3a

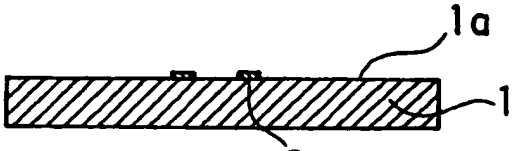


FIG. 3b

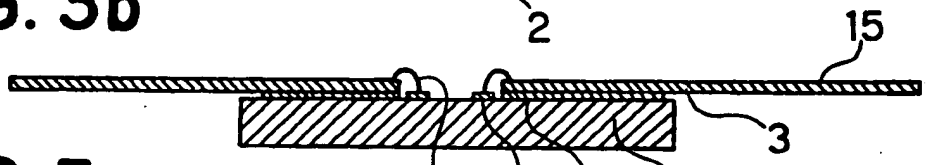


FIG. 3c

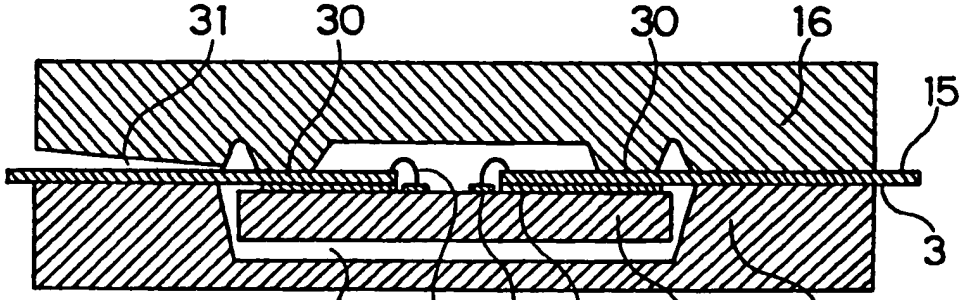


FIG. 3d

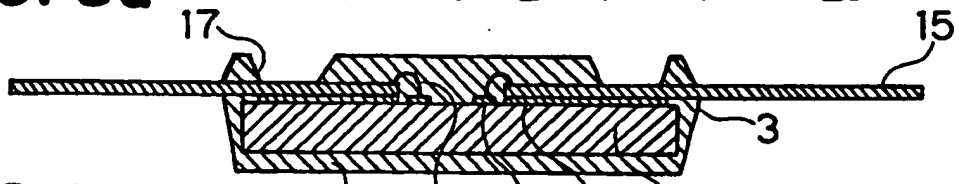


FIG. 3e

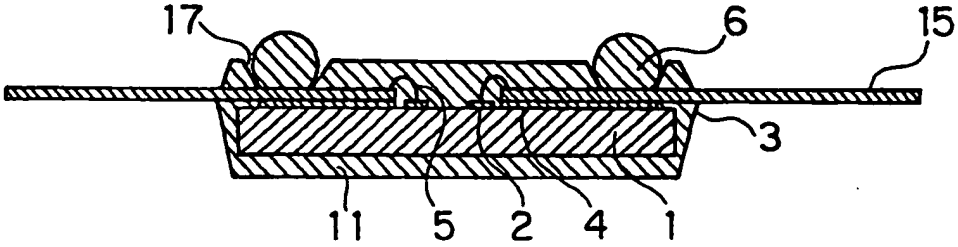


FIG. 3f

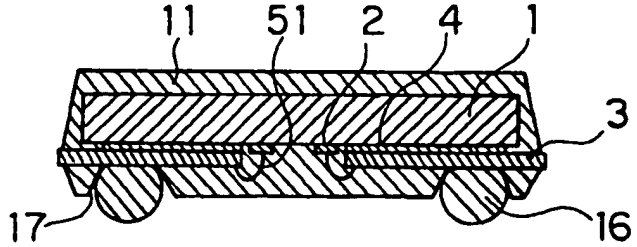


FIG. 4

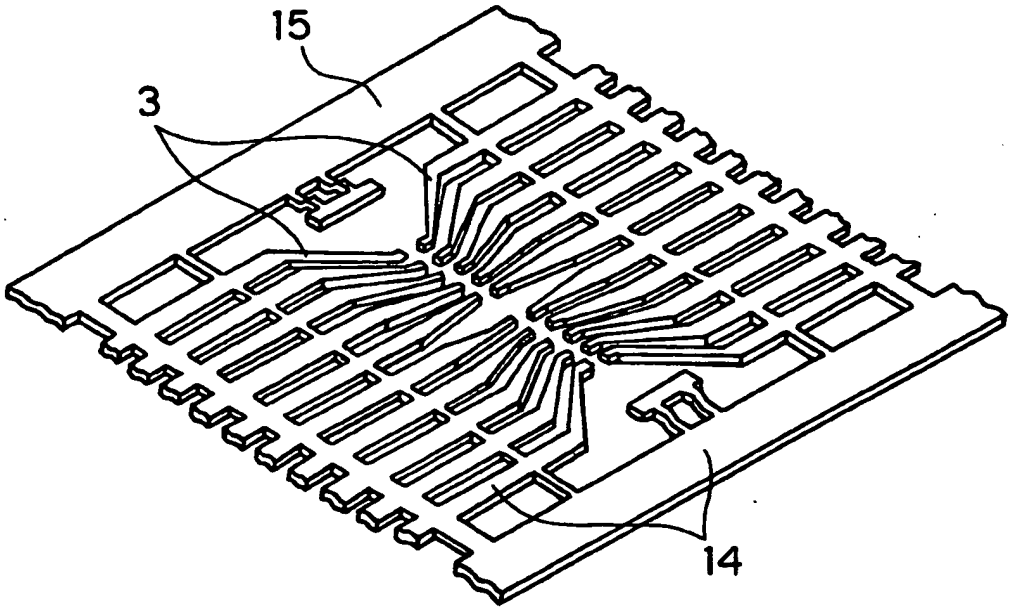


FIG. 5

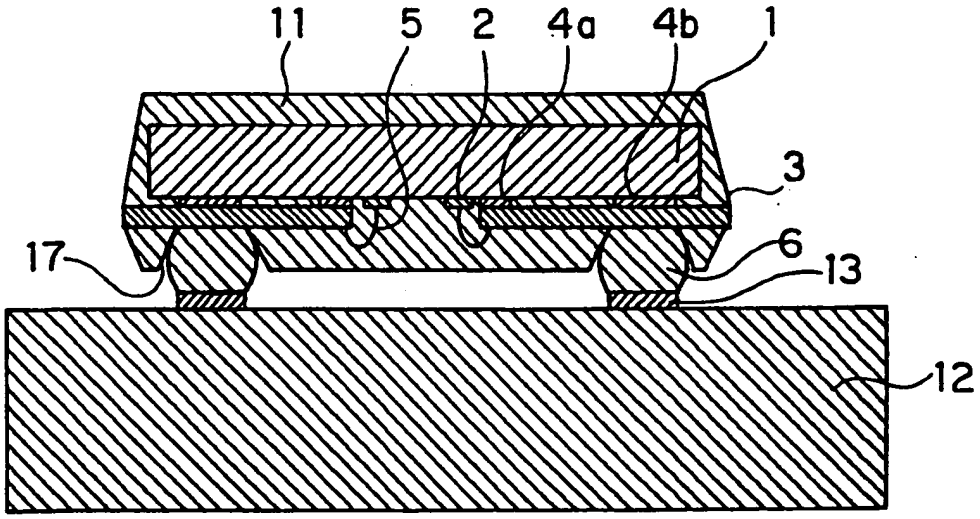


FIG. 6

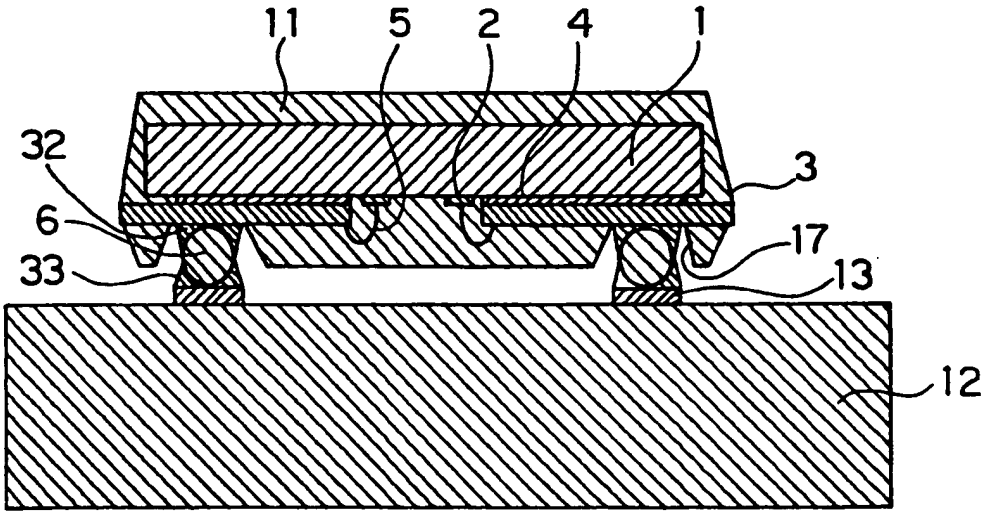


FIG. 7

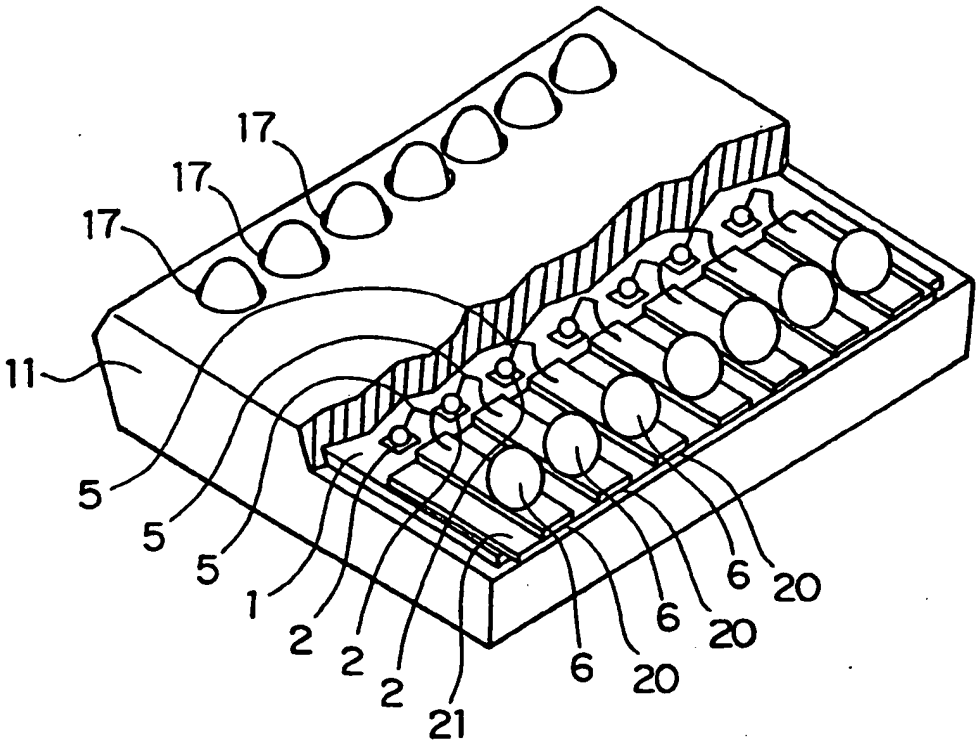


FIG. 8

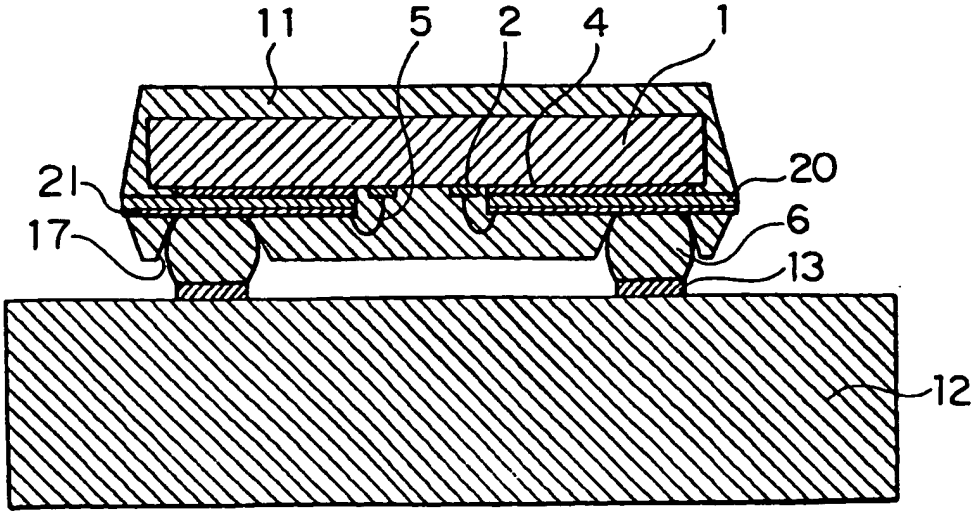


FIG. 9

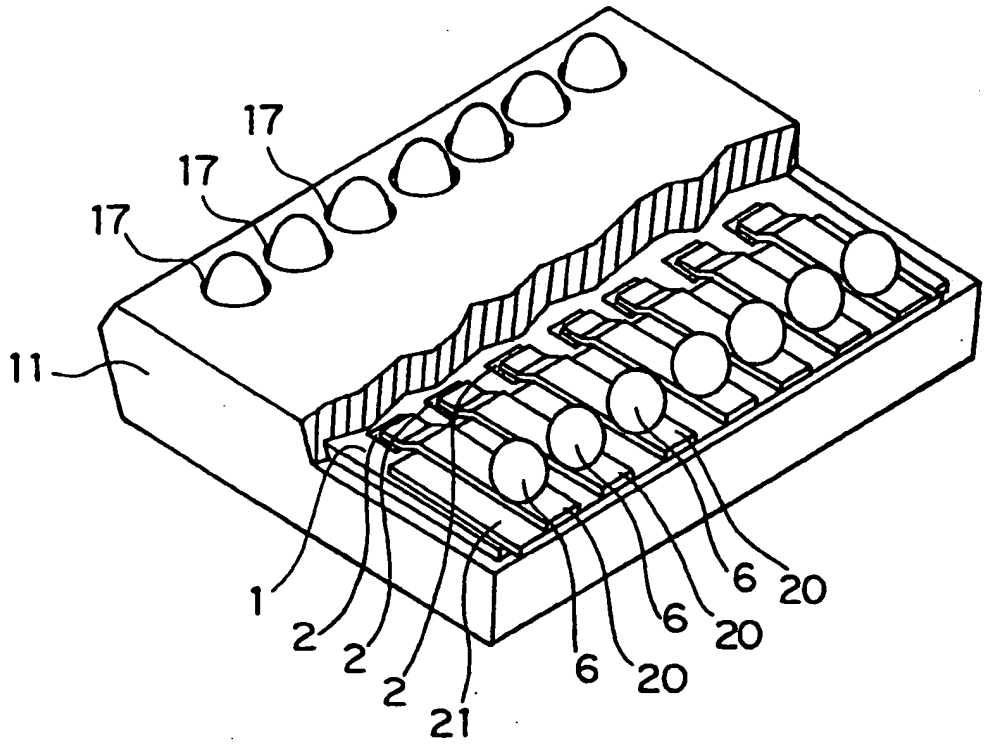


FIG. 10

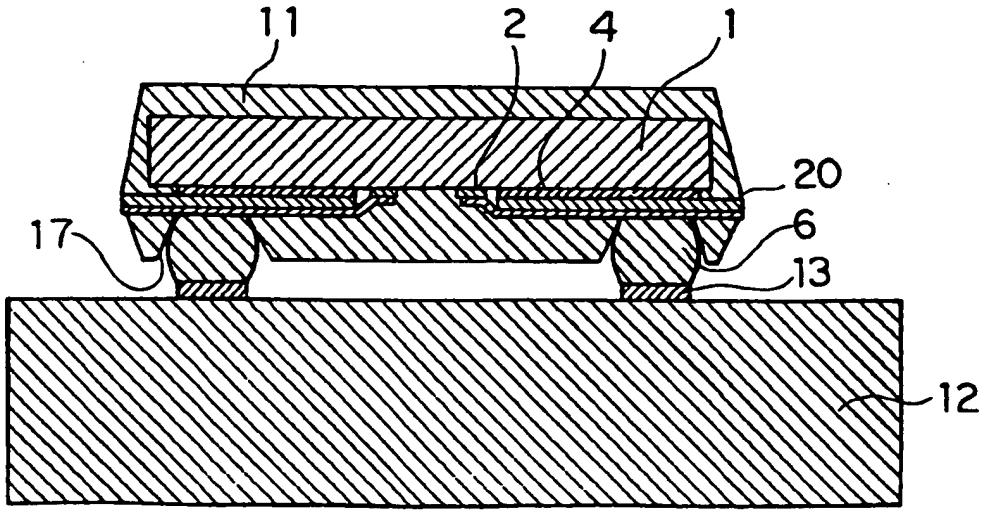


FIG. 11

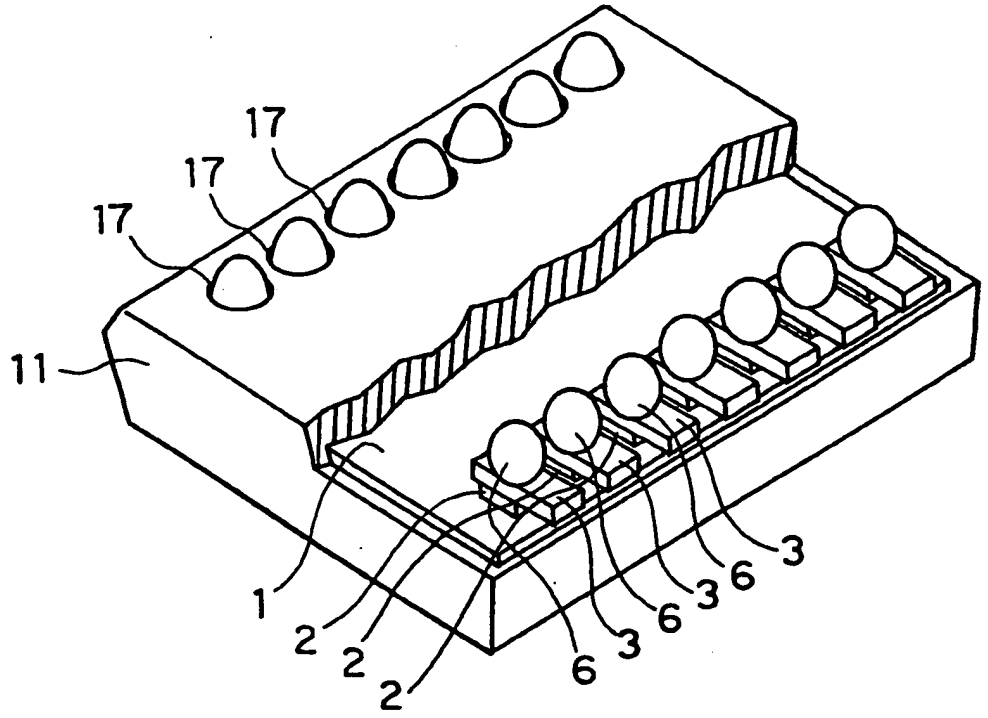


FIG. 12

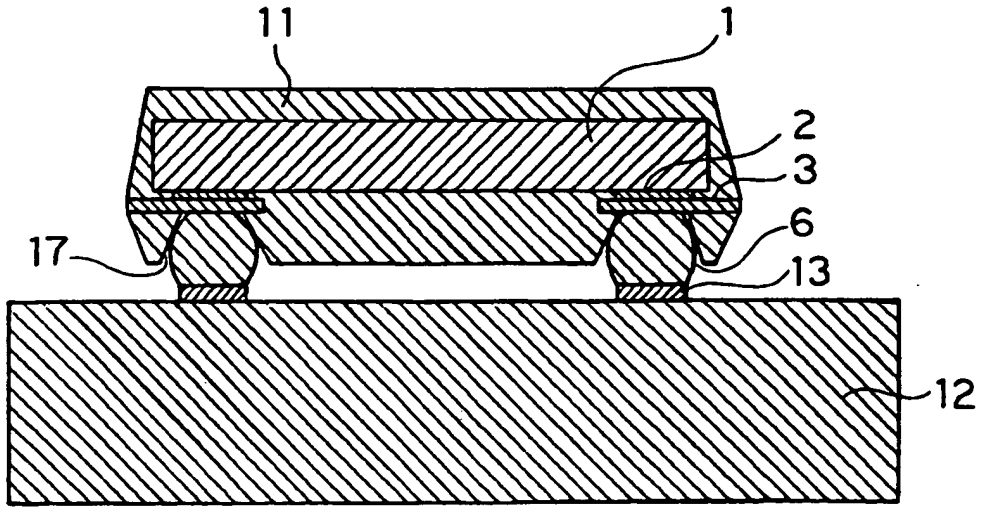


FIG. 13

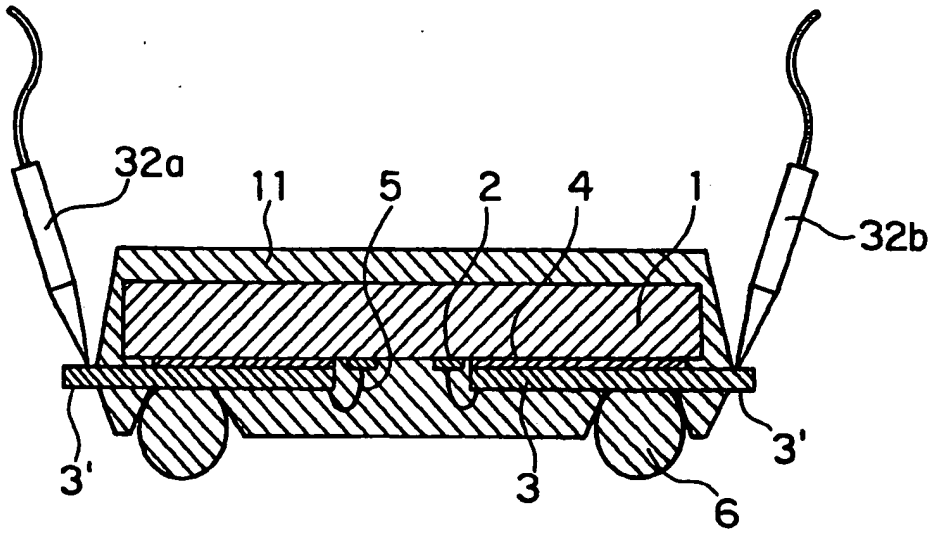


FIG. 14

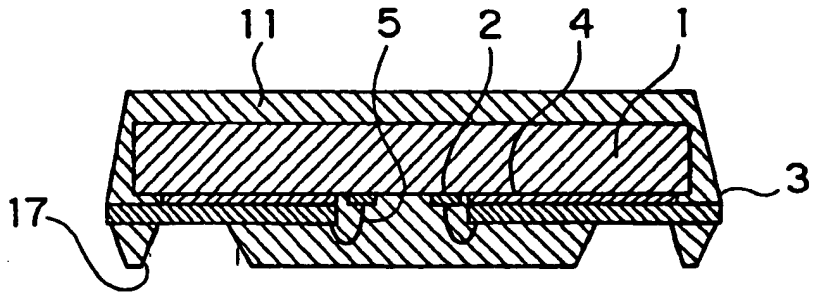


FIG. 15

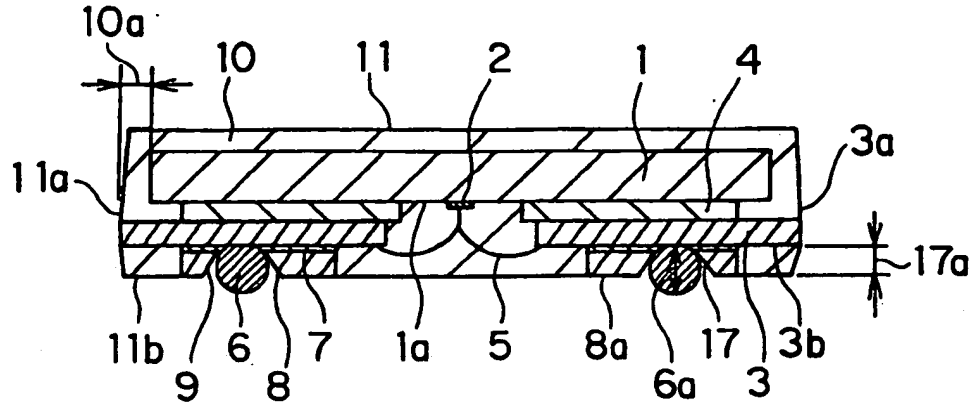


FIG. 16

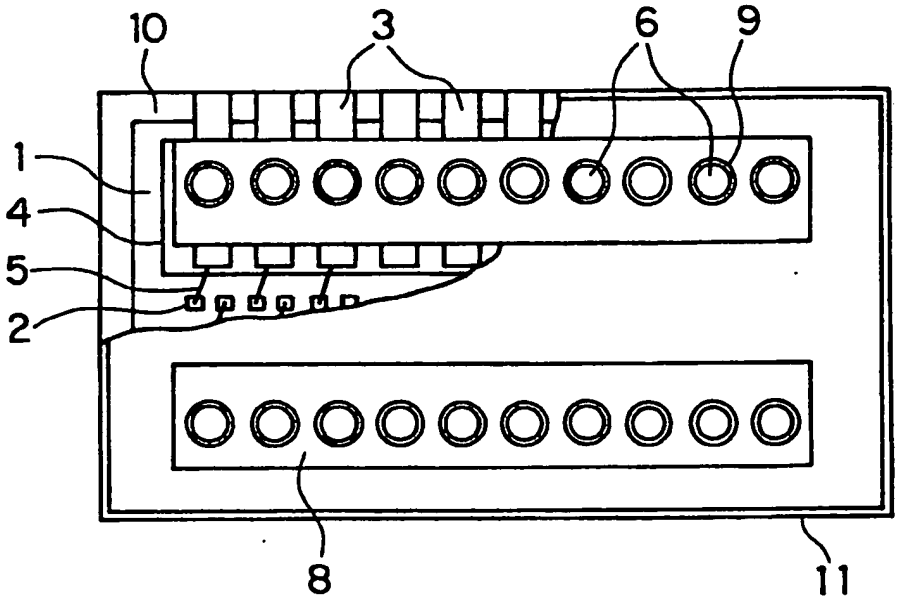


FIG. 17

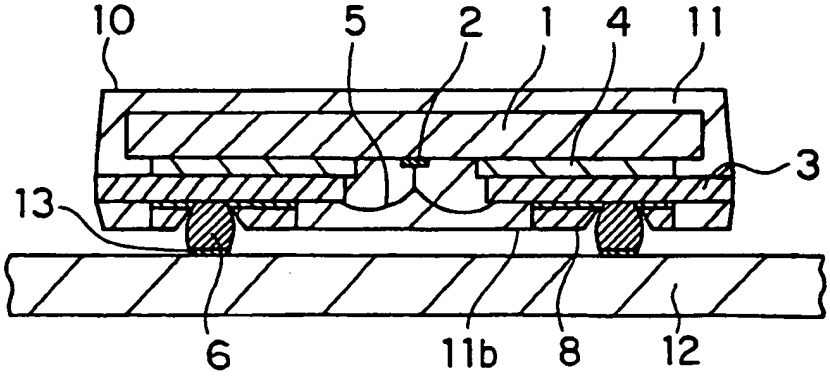


FIG. 18a

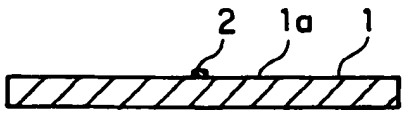


FIG. 18b

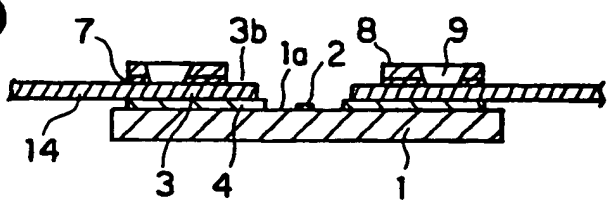


FIG. 18c

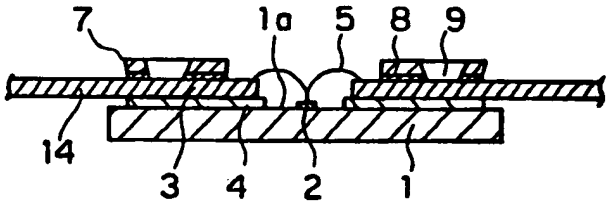


FIG. 18d

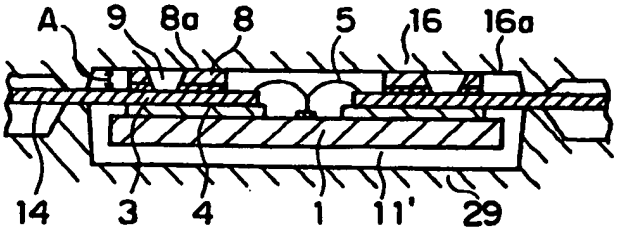


FIG. 18e

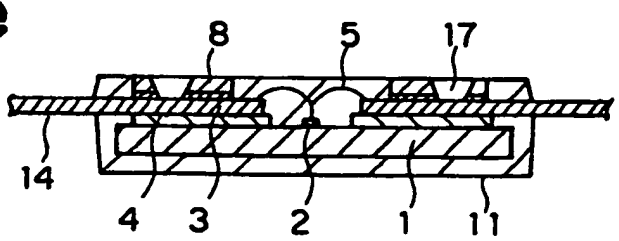


FIG. 18f

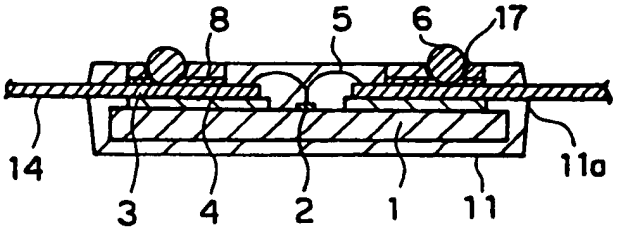


FIG. 18g

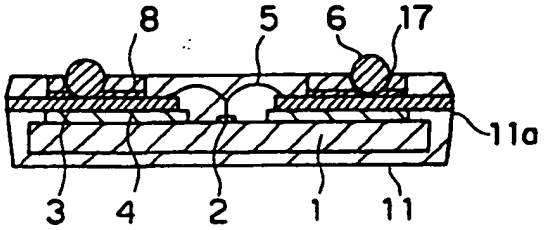


FIG. 19a

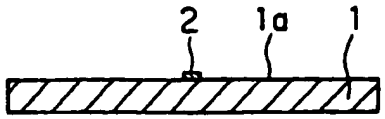


FIG. 19b

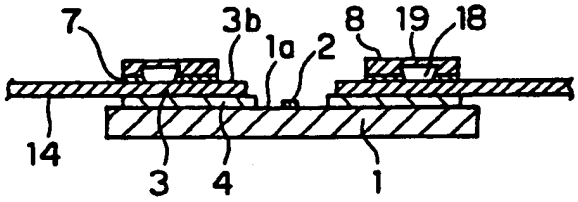


FIG. 19c

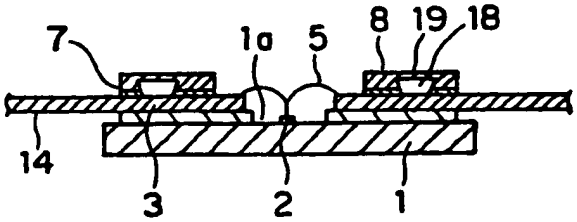


FIG. 19d

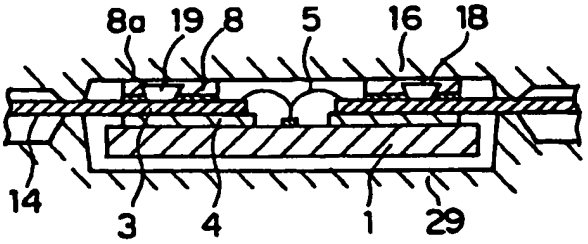


FIG. 19e

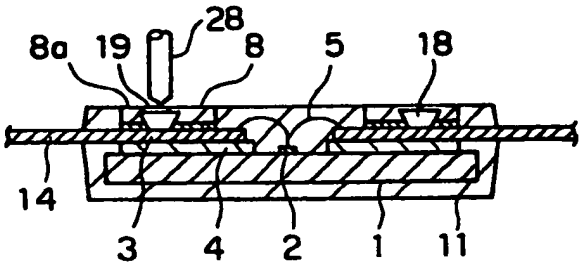


FIG. 19f

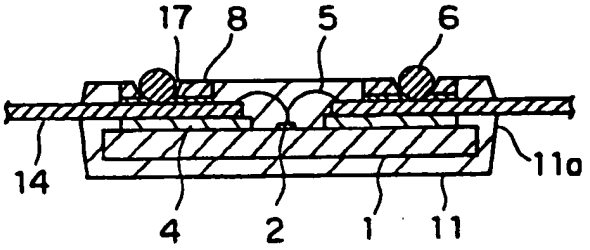


FIG. 19g

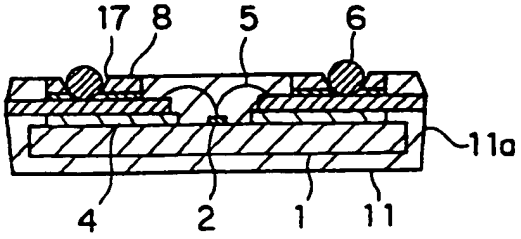


FIG. 20

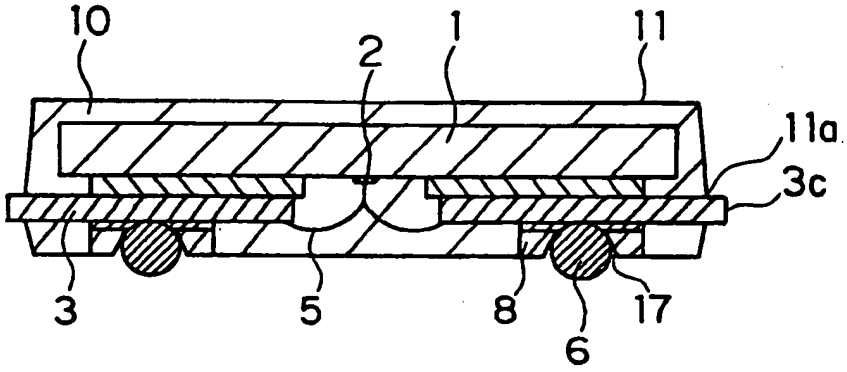


FIG. 21

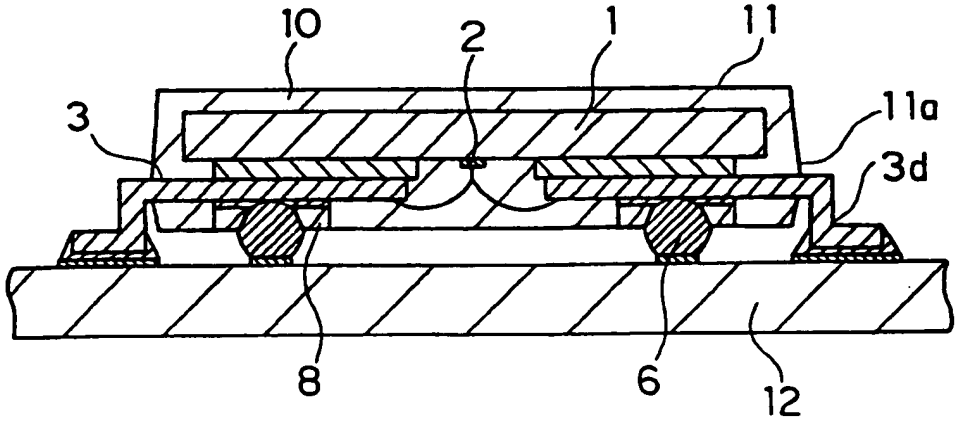


FIG. 22

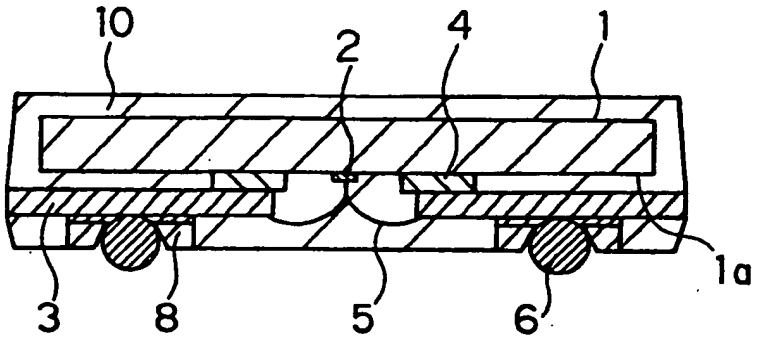


FIG. 23

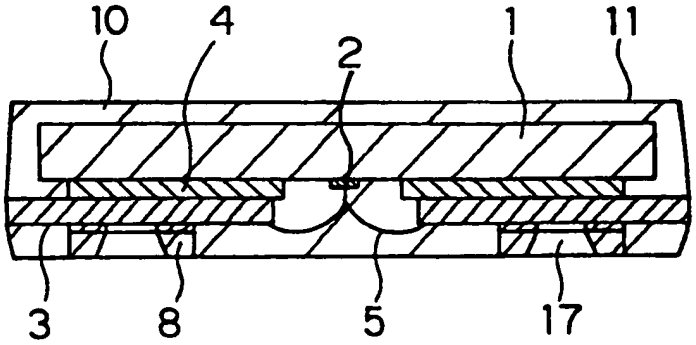


FIG. 24

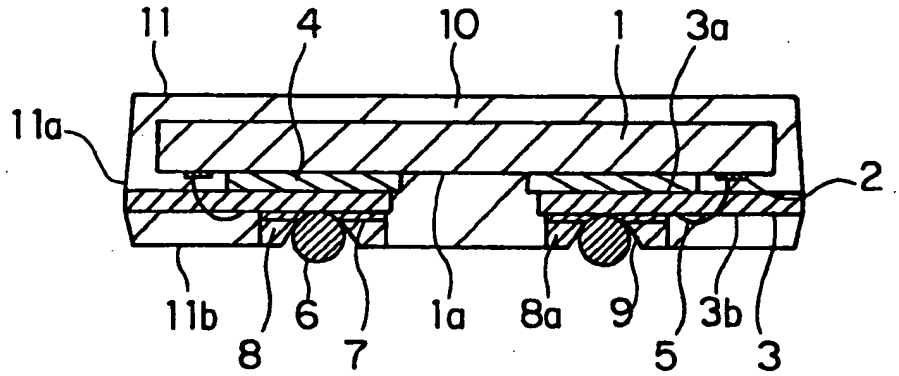


FIG. 25

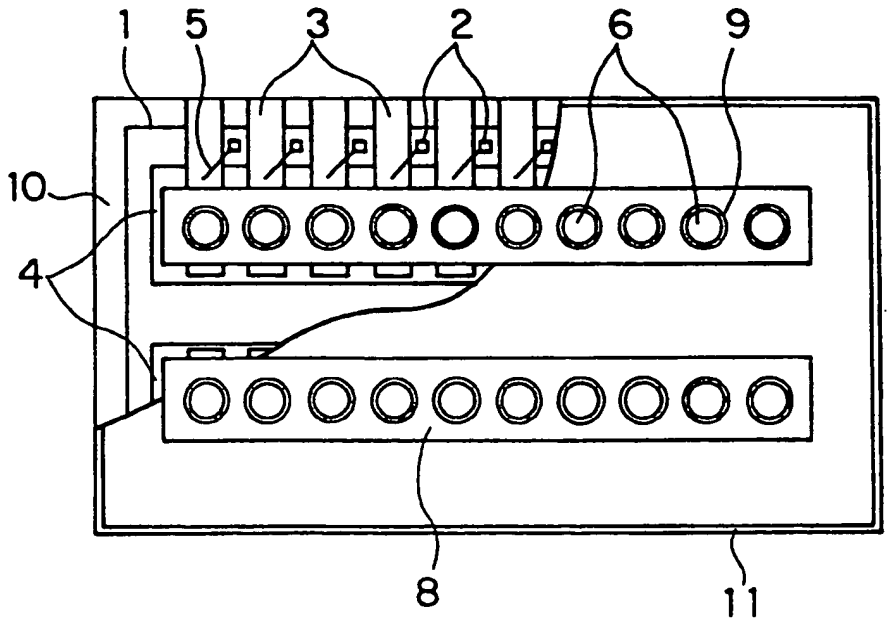


FIG. 26

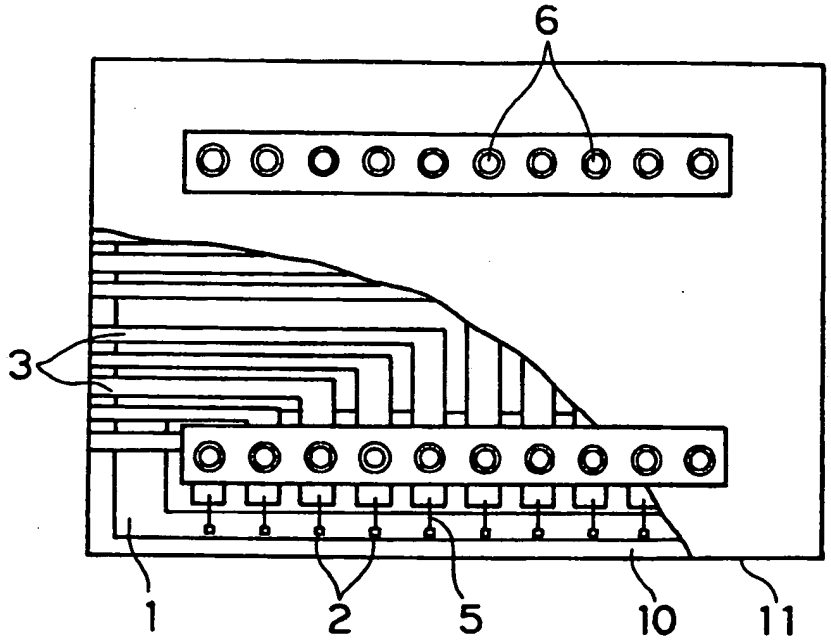


FIG. 27

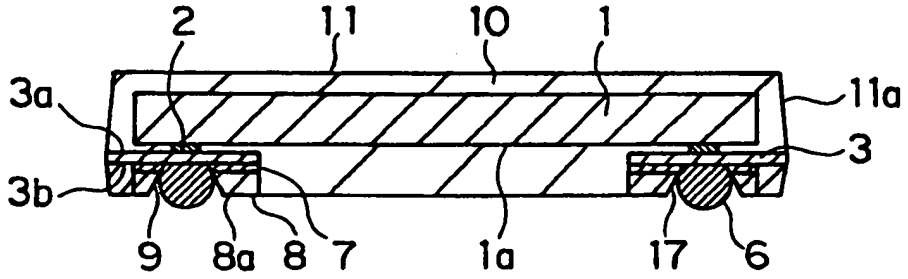


FIG. 28

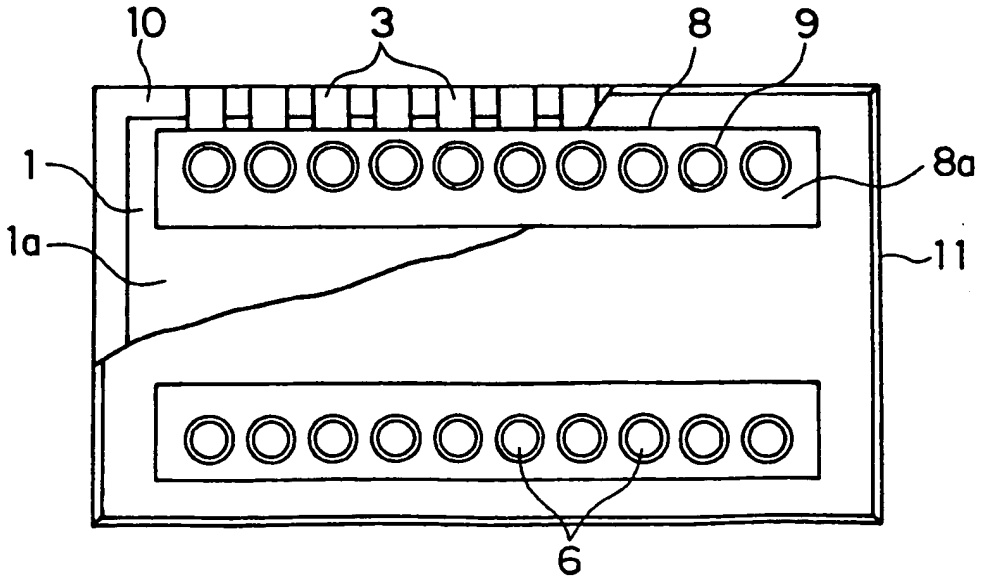


FIG. 29

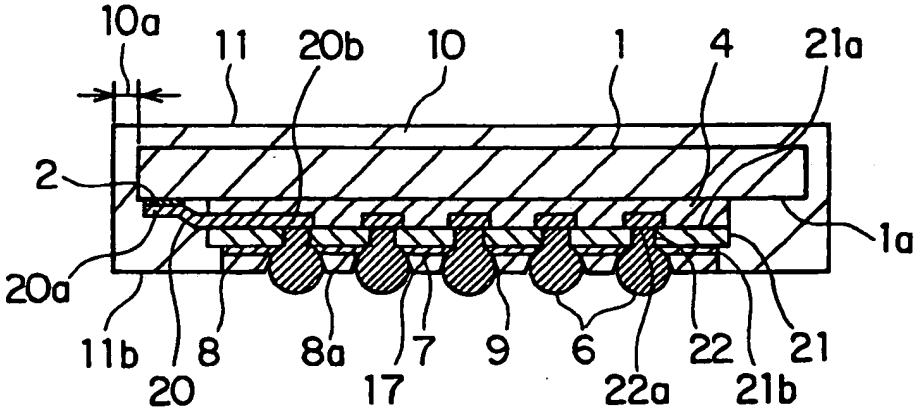

10a
11
20b
10
1
4
21a
2
1a
20a
11b
20
8
8a
17
7
9
6
22a
22
21b
21

FIG. 30

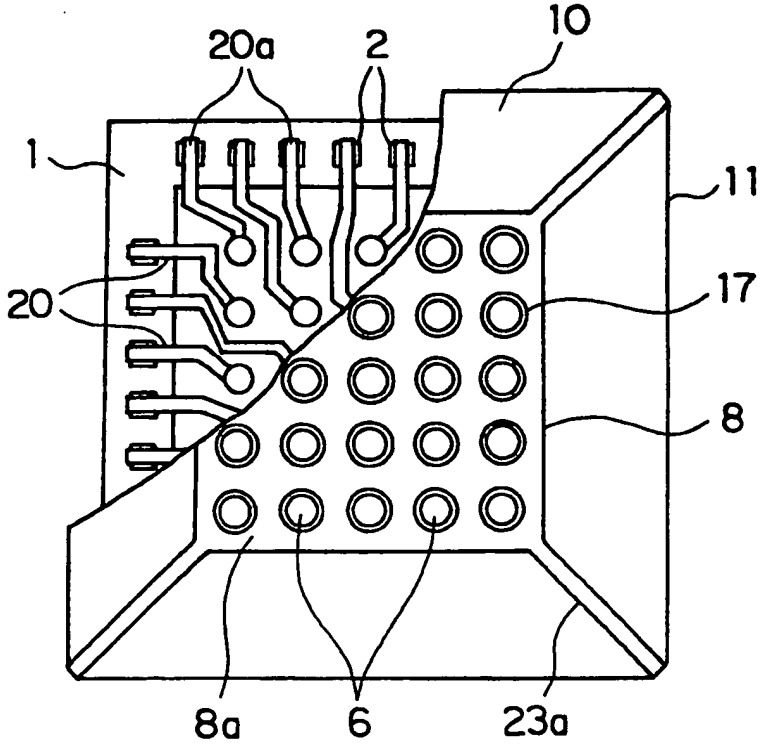

20a
2
10
1
11
20
17
8
8a
6
23a

FIG. 31a

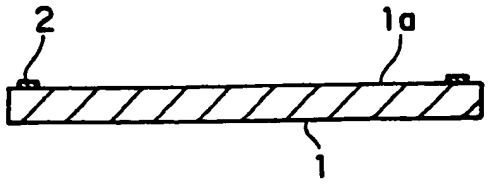


FIG. 31b

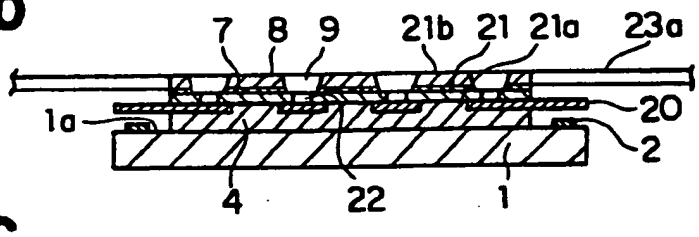


FIG. 31c

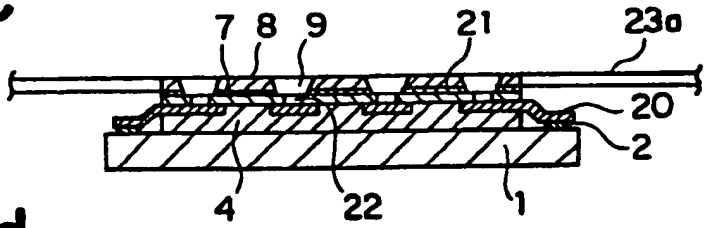


FIG. 31d

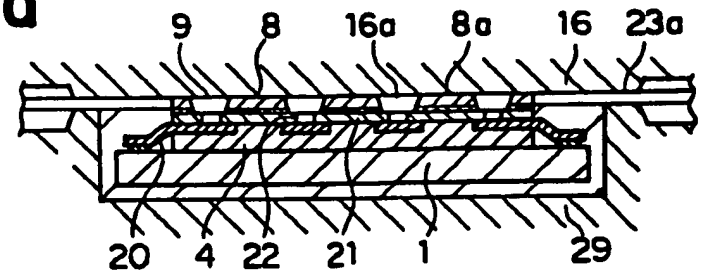


FIG. 31e

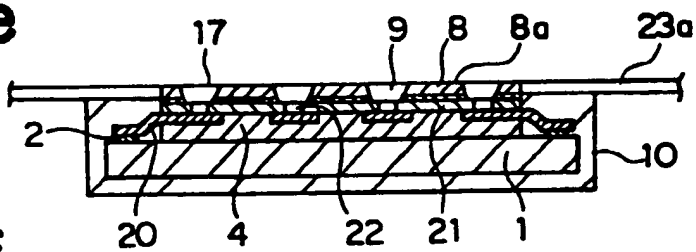


FIG. 31f

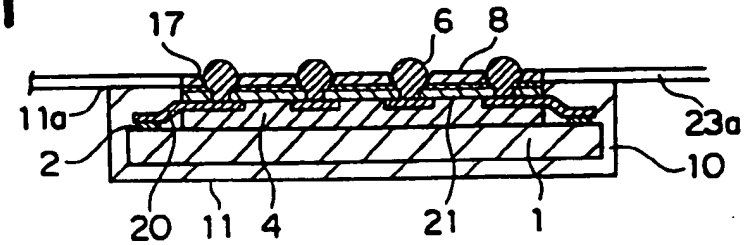


FIG. 31g

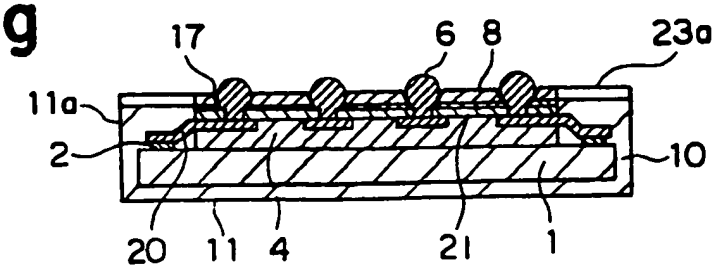


FIG. 32

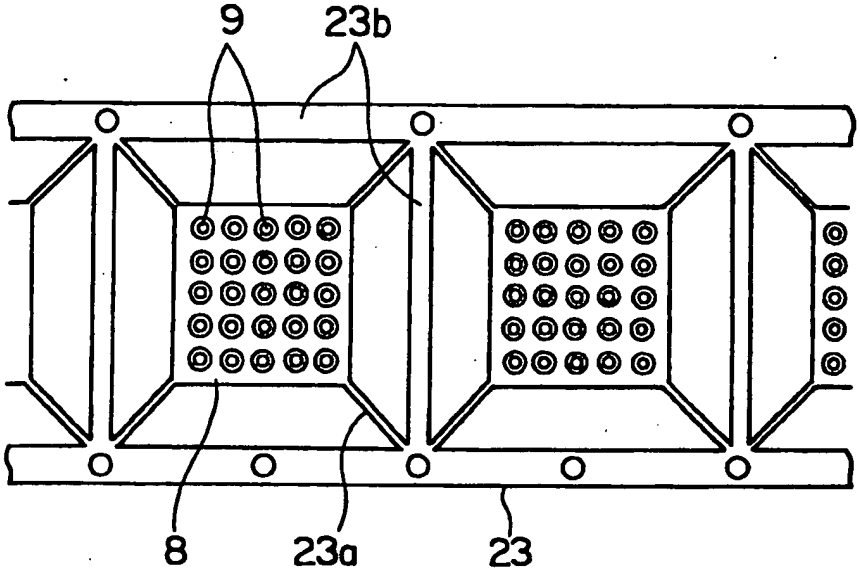


FIG. 33

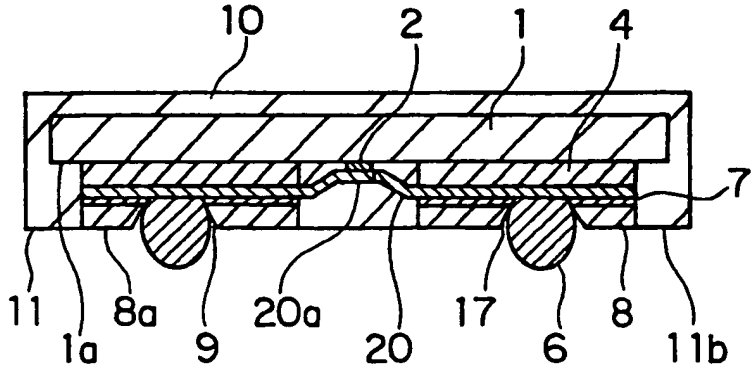


FIG. 34

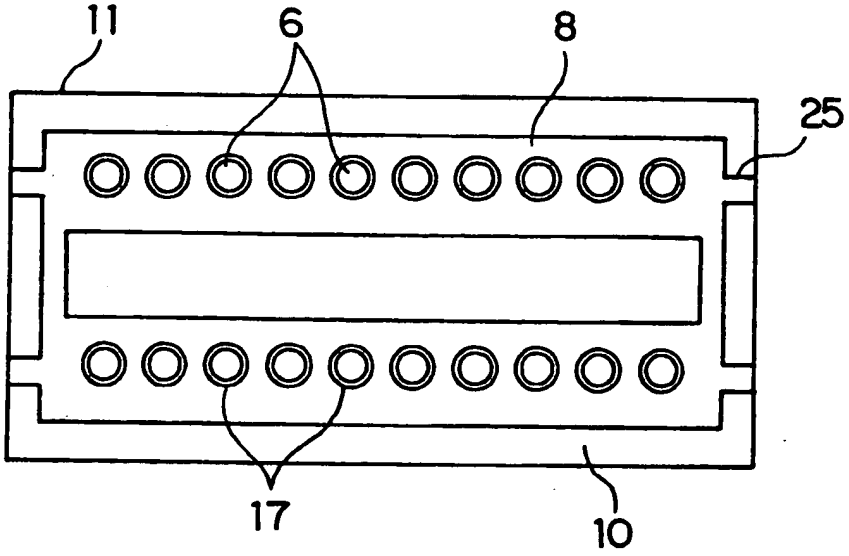


FIG. 35

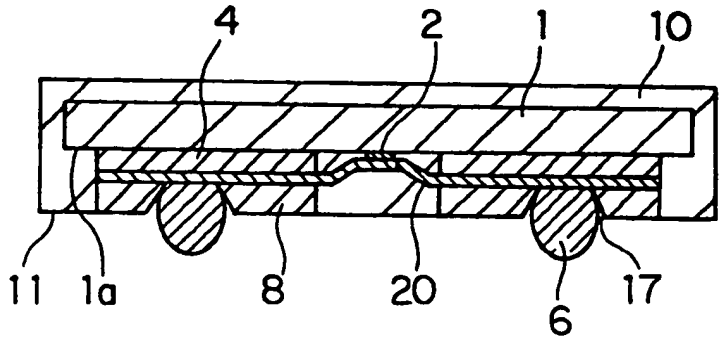


FIG. 36

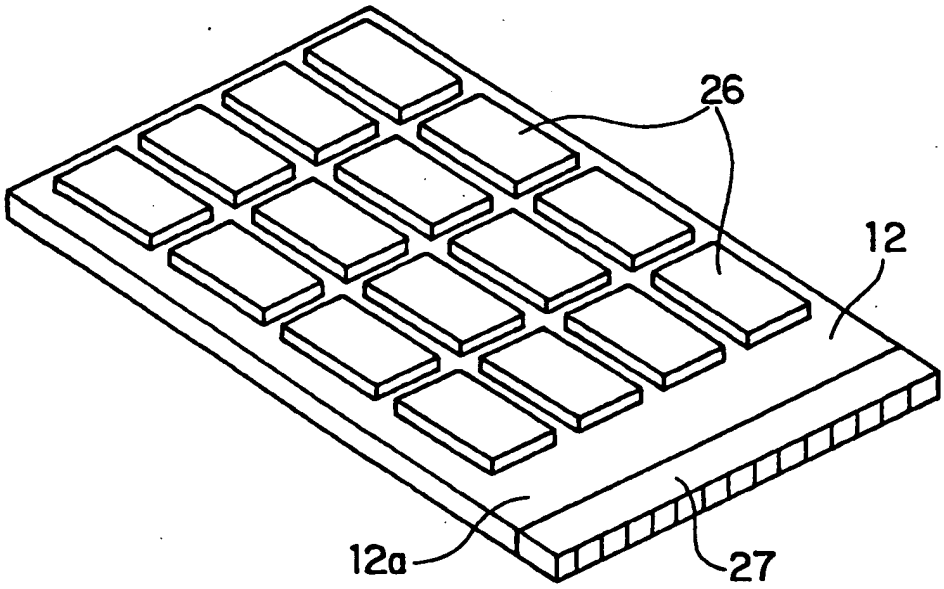
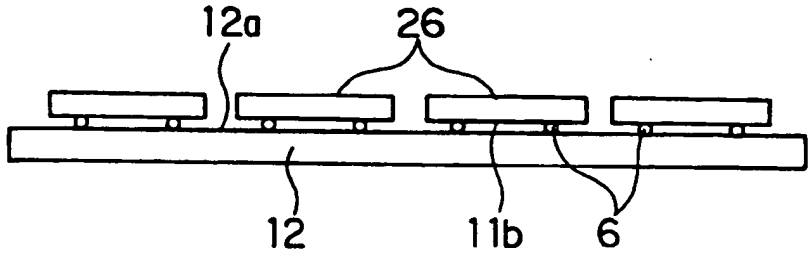


FIG. 37



INTERNATIONAL SEARCH REPORT

Intern[illegible]al Application No
PCT/JP 96/01689

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/495 H01L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 673 (E-1647), 19 December 1994 & JP,A,06 268101 (HITACHI LTD), 22 September 1994, cited in the application	1,4-6, 8-11, 15-18, 20,23
Y	see the whole document	21
P,X	DE,A,195 26 511 (MITSUBISHI ELECTRIC CORP) 25 January 1996	1,4-6, 8-12, 16-18
P,A	see column 9, line 37 - column 12, line 29; figures 1-8	20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 August 1996	17.09.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Zeisler, P

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 403 (E-1584), 27 July 1994 & JP,A,06 120296 (HITACHI LTD;OTHERS: 01), 28 April 1994,	1,2,5,9, 15-18
Y	see abstract	21
A		24

A	PATENT ABSTRACTS OF JAPAN vol. 94, no. 010 & JP,A,06 302604 (MITSUBISHI ELECTRIC CORP), 28 October 1994, cited in the application see the whole document	1,5,6,8, 9,15

1

INTERNATIONAL SEARCH REPORT

...ormation on patent family members

Interna...nal Application No
PCT/JP 96/01689

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE-A-19526511	25-01-96	JP-A- 8037253	06-02-96